Baseband Signal Processing Technologies for 64 Mbit/s Radio Transmission for Mobile Broadband Systems

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Abstract: *This paper proposes a novel scheme of baseband signal processing technologies that mainly contains an equalisation scheme and a TDMA slot and frame synchronisation scheme to be operated at 64 Mbit/s radio transmission for mobile broadband systems.*

1. Introduction

The future Mobile Broadband System (MBS) will feature the transport of Asynchronous Transfer Mode (ATM) cells over the air interface in order to provide to the mobile user access to the future Broadband ISDN (B-ISDN) fixed networks.

The SAMBA (System for Advanced Mobile Broadband Applications) project is working within the scope of the future MBS. The target of SAMBA is to provide a Trial Platform for the demonstration of fully mobile interactive broadband applications up to 34 Mbit/s at the EXPO '98 in Lisbon.

The Trial Platform will operate in the 40 GHz frequency band (one of the frequency band provisionally allocated for MBS) to enable high data rates in indoor and outdoor environments. It will demonstrate broadband communications in TDMA mode (Time Division Multiple Access) and handover with a mobile velocity up to 50 km/h. Therefore, the technical constraints for the air interface are the characteristics of the transmission channel (rms delay spread, delay window, Doppler influence) and also the free mobility of the users (velocity, omnidirectionnal antennas for the mobile and handover capability).

We have been engaged in making research and development on baseband signal processing technologies for future mobile communication systems, and the results are applied to the SAMBA project.

The key issues to be coped with in the baseband signal processing unit (BBPU) are as follows:

(1) New equalisation technology to compensate large delay spread and frequency-selective fading.

(2) New fast synchronisation technology in TDMA mode operation.

This paper describes the design concept of the BBPU and some key technologies such as an adaptive equalisation and TDMA functionality including the synchronisation scheme. All these functions are performed in the Baseband Processing Unit by ASICs operating at the maximum speed of 64 Mbit/s.

2. Overall Concept and Scheme of the Baseband Signal Processing Unit

In order to define the functionality of the BBPU, air interface requirements and a channel profile model have been determined. The slot and frame structures and some key transmission parameters (each burst transports 2 ATM cells: PL1 + PL2 + PL3 + PL4 = 2 ATM cells, TS: training sequence, TX: tail sequence) are shown in Figure 1[1]. Because of the redundancy required (for coding,

equalisation, signalling ...), a gross bit rate of 64 Mbit/s is necessary to achieve a user information bit rate of approximately 34 Mbit/s. The digital modulation used is offset QPSK(OQPSK), hence the modulation rate over the air interface is 32 MBaud (1 symbol period is 31.25 ns).

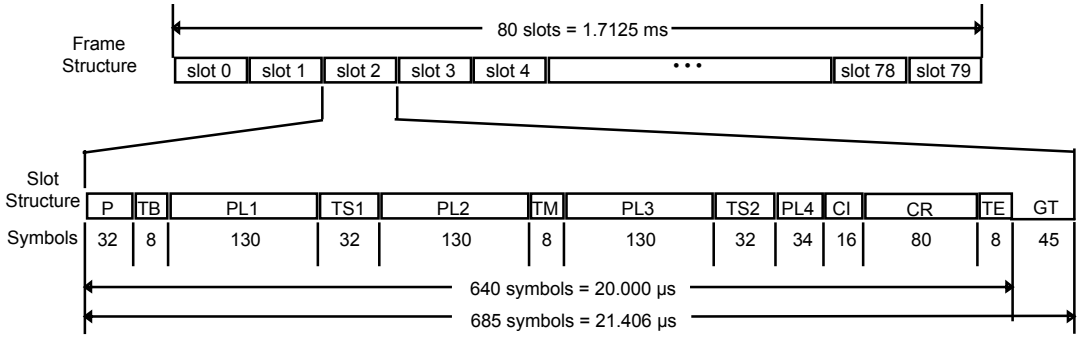

Figure 1. Slot and frame structures

A typical channel model for the EXPO '98 has been derived through ray tracing technique. In this model the maximum delay spread is around 250 ns, which corresponds to 8 transmission symbols, and the two diversity branches are assumed to be uncorrelated [2].

Under these conditions the required performance target for the bit error rate (BER) for the specified channel model is less than 5.0×10^{-3} at the output of the equaliser. In order to attain these performance requirements, the following functions are fulfilled by the BBPU:

(1) Achievement of the signal quality (BER performance) under the specified channel model with large delay spread.

(2) Fast acquisition and maintaining slot synchronisation of the received signal in the burst mode transmission.

When designing the BBPU, the following main features have been considered:

- Diversity reception
- Equaliser scheme and channel impulse response estimation
- Automatic Gain Control (AGC) for received burst signal
- Slot synchronisation

The overall functional block diagram of the BBPU in development is shown in Figure 2.

On the transmit side the data stream coming from the FEC (Forward Error Correction) encoder is passed to the framing circuit in order to generate the TDMA burst containing 2 ATM cells as indicated in Figure 1. Then, in the OQPSK mapping circuit, each 2-bit pair is mapped to an OQPSK symbol, which is provided to the analogue I/Q modulator after D/A conversion.

At the receive side signal processing is applied to the received baseband signal in order to produce the data stream for the FEC decoder. Each received signal from the two diversity branches is A/D converted, and then supplied to the TS (Training Sequence) detector followed by the equaliser, the retiming circuit, and the deframing circuit. In the TS detector correlation detection is done between the local replica of the TS and the received baseband signal before equalisation to achieve both fast initial synchronisation and fast re-synchronisation after blockage due to fading.

In the equaliser the signal processing is done in a parallel configuration to cope with high-speed signal transmission. The received signal distortion due to multipath fading is equalised and the maximal-ratio combining of the two diversity branches is also done to achieve specified signal quality, as explained in detail in Section 3. The slot synchronisation is acquired and is maintained in the TX/RX

timing management circuit and the slot synchronisation circuit, as also explained in Section 3. In the deframing circuit information is extracted from each burst, and is provided to the FEC decoder.

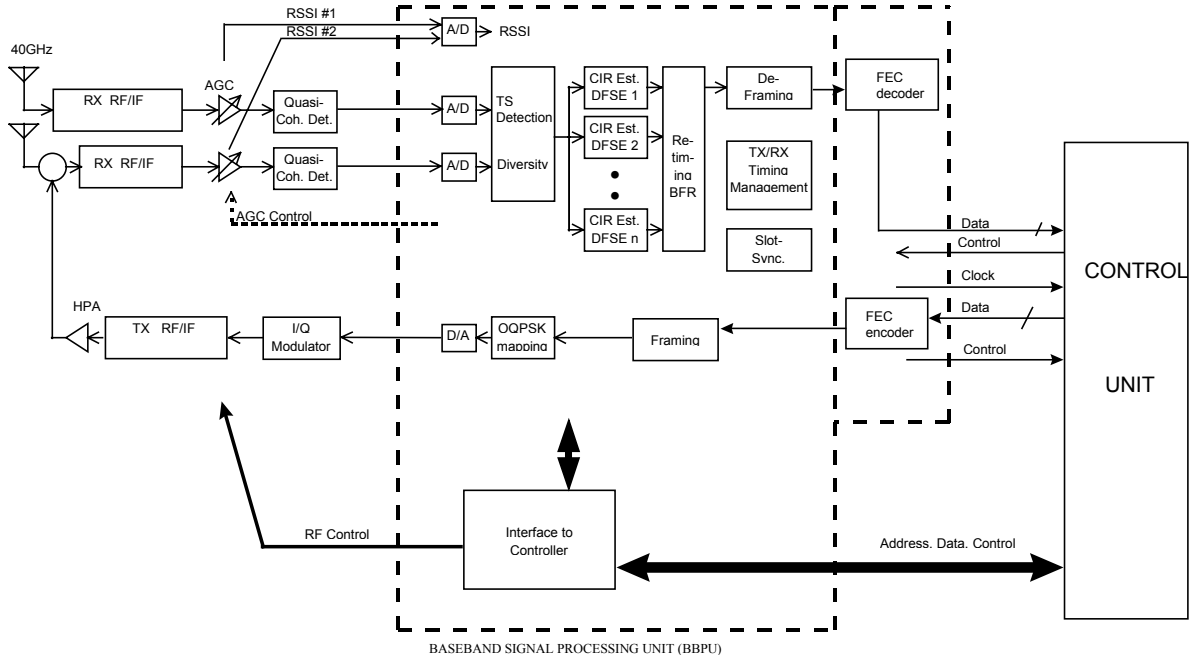

Figure 2. Overall functional block diagram of the BBPU

3. Key Technologies and Performance

3.1 Equalisation with Diversity Reception

Several equalisation schemes have been studied, e.g., Viterbi equalisation and decision-feedback equalisation. It is well-known that maximum-likelihood sequence estimation (MLSE), which is a class of Viterbi equalisation, is the optimal receiver in the presence of intersymbol interference (ISI). However, its complexity increases exponentially with the channel memory length. Therefore, the other class of Viterbi equalisation, e.g., decision-feedback sequence estimation (DFSE), is suitable for the MBS environments.

The equaliser for the SAMBA project is a modified version of a DFSE with maximum-ratio diversity combining in order to reduce hardware complexity. Its equalisation span is 8 symbols and its aperture width for detection of each TS is ± 7 symbols. Figure 3 shows the configuration of the equaliser. In this equaliser the channel/timing estimator estimates both sampling timing and channel impulse response (CIR) for each diversity branch. The DFSE operates based on the Viterbi algorithm by using these timings and CIRs as reference for the survivor paths for its branch metric generation.

The basic operation of this equaliser using the slot structure of Figure 1 is as follows:

(1) Estimation of the CIR by means of training sequences TS1 and TS2.

(2) Detection of the data of PL1 and PL2 based on the CIR estimated by TS1, where equalisation for PL1 and PL2 is initialised by TB and TS1, respectively.

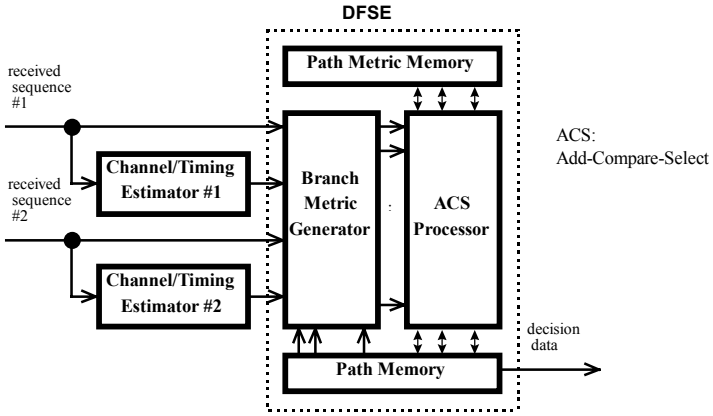

Figure 3. Configuration of the adaptive equaliser

(3) Detection of the data of PL3 and PL4 (including CI and CR) based on the CIR estimated by TS2, where equalisation for PL3 and PL4 (including CI and CR) is initialised by TM and TS2, respectively.

Table 1 shows computer simulation conditions, other conditions are assumed to be ideal.

Table 1. Simulation Conditions

Item	Condition
mobile velocity	50 km/h
transmission bit rate	64 Mbit/s
carrier frequency offset	± 0.1 ppm
channel conditions	i) AWGN channel ii) Fading channel model of the EXPO '98
average E_b/N_0	average E_b/N_0 in each diversity branch
slot structure	see Figure 1
AGC control	frozen during equaliser's operation

Figures 4 and 5 show the BER performance obtained by computer simulation in various channel conditions. Figure 4 shows the BER performance on the AWGN channel and Figure 5 shows that on the fading channel specified for the EXPO '98 environment. These figures show that the proposed equaliser can cope with severe signal distortions caused by wide-spread time-dispersive channels.

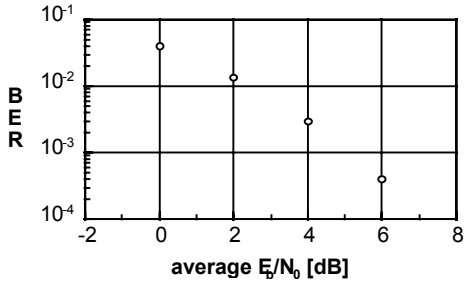

Figure 4. BER on AWGN channel

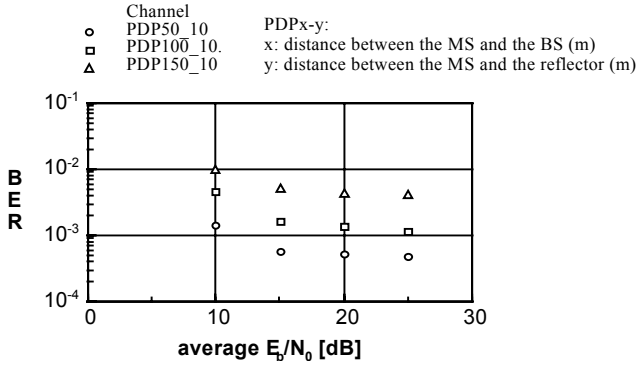

Figure 5. BER on fading channel

3.2 Slot Synchronisation

The main feature of the slot synchronisation scheme is the timing management of transmission and reception based on TS detection and a flywheel counter. There is some frequency deviation between base station (BS) and mobile terminal (MT). Therefore, the MT always has to track the slot timing of the BS. The slot synchronisation will be implemented with the following functions:

- Averaging of the received slot timing and control of the aperture window to prevent from false detection of the TS.
- Maintenance of the slot synchronisation during deep fading caused by obstructed line-of-sight (LOS) paths.

The functional block diagram of TDMA slot synchronisation for an MT is shown in Figure 6.

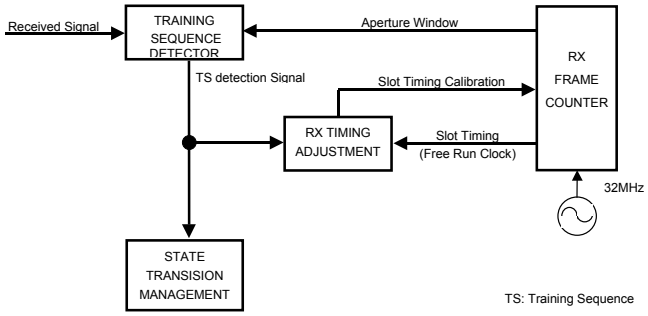

Figure 6. Basic concept of TDMA slot synchronisation for the MT

The BBPU detects the known TS in the received burst signal and determines the start symbol of each burst.

The BBPU will employ a slot synchronisation scheme based on a flywheel mechanism, where synchronisation information for the previous bursts is retained and updated for the current burst synchronisation.

Slot synchronisation management is based on the state transition scheme shown in Figure 7. The following is a description of respective states N1and N2 are positive integers.

Out-of-Synchronisation (Out-of-Sync) State

When the Mobile Terminal is powered on, the BBPU first stays in the Out-of-Sync state. The whole received burst is then searched for a TS. In other words, an open window mode is used.

Synchronisation-Protection B (Sync-Protection B) State

When the TS is detected and the burst is declared valid, the state is transferred to the Sync-Protection B State. In this state, a reduced size window is used for TS detection, i.e. a limited part of the burst is scanned for the TS. The position of the window is determined by averaging the previous TS positions. If TS miss-detection occurs, the state is transferred to the Out-of-Sync state, and if N2 consecutive TS detections with a valid burst occur, the state is transferred to the In-Sync state.

In-Synchronisation (In-Sync) State

This corresponds to the state, where the bursts are detected and declared valid. However, when a TS is not detected, the state is transferred to the Sync-Protection F state.

Synchronisation-Protection F (Sync-Protection F) State

Although the TS is not detected in this state, synchronisation is still being kept and the bursts are declared valid. Once a TS is detected again, the state is transferred to the In-Sync state. However, this state can not be kept for more than N1 bursts. When the TS in consecutive N1 bursts is not detected, the state is transferred to the Out-of-Sync state.

In the base station slot synchronisation has to be maintained for the communication with each mobile terminal.

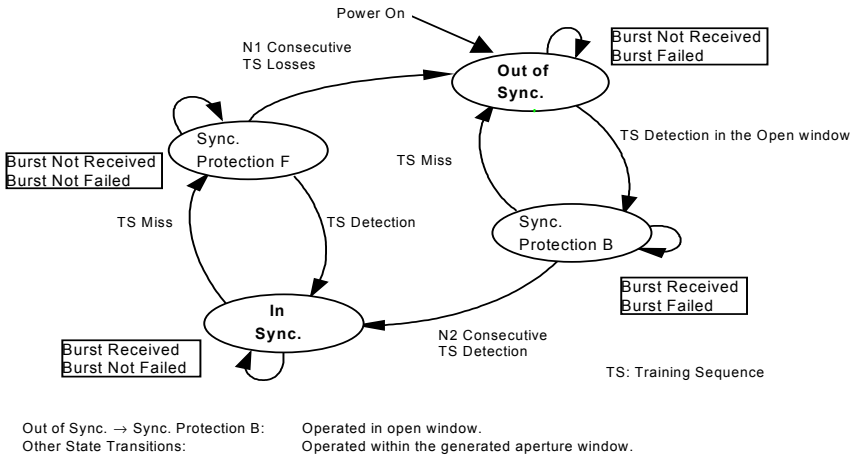

Figure 7. Slot synchronisation management based on state transition diagram for the MT

The performance evaluation of the slot synchronisation process, such as false-detection and mis-detection probabilities of the TS, is carried out by computer simulation, and parameters N1 and N2 will be determined in accordance with this evaluation.

4. Conclusions

The design concept and some key technologies of the baseband signal processing unit for the SAMBA Trial Platform have been described. The equalisation scheme using a modified version of DFSE with maximum-ratio diversity combining has been investigated and was confirmed to produce a sufficient performance under the prescribed channel model. The slot synchronisation scheme, indispensable for high speed TDMA operation, has also been investigated and design parameters will be determined after detailed performance evaluation. These technologies are essential for baseband signal processing for Mobile Broadband Systems. On the basis of this design concept the implementation of the BBPU is now being executed.

Acknowledgement

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References

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