Design of Baseband Signal Processing Unit in SAMBA Trial Platform for Mobile Broadband Applications

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Abstract: The target of SAMBA is to develop a Trial Platform for the demonstration of fully mobile interactive broadband applications up to 34 Mbit/s. The baseband processing unit (BBPU) performs functions of modulation/demodulation, TDMA signal processing and Forward Error Correction. This paper, following the previous paper [2], describes the design concept and implementation features of the BBPU together with some test results.

1. Introduction

The SAMBA (System for Advanced Mobile Broadband Applications) project is working within the scope of the future MBS (Mobile Broadband System) [1]. The Trial Platform will operate in the 40 GHz frequency band, one of the frequency band provisionally allocated for MBS, to enable high data rates in indoor and outdoor environments. Single carrier modulation is employed to mitigate the requirement on powerful broadband linear power amplifiers. SAMBA aims at broadband communications in time division multiple access (TDMA) mode, and handover with a mobile velocity up to 50 km/h.

Mobile broadband signal transmission has to cope with environment of transmission channel with large delay spread and frequency-selective fading. Equalisation technology based on Decision Feedback Sequence Estimation (DFSE) is developed and employed. Another key technology is TDMA functionality including slot synchronisation. Design of the BBPU is completed, and hardware testing is commenced.

2. Overall Design

2.1 BBPU Specification

The specification of the air interface of the SAMBA Trial Platform is summarized in Table 1 [1]. The frame format and the transmission parameters are as shown in Fig. 1.

Table 1. Summary of specifications for SAMBA Air Interface

Item	Condition
Carrier frequency	40 GHz
Multiple access	TDMA/FDD
Modulation	OQPSK
Transmission bit rate	64 Mbit/s
Max. ATM cell bit rate	34 Mbit/s
Terminal mobility	Up to 50 km/h
Base station antennas	two types of directional antennas for wide and elongated cells
Portable terminal antenna	Omni directional (azimuth) for full mobility
Frame format	See Fig. 1
Channel model	Max. delay up to 250 ns

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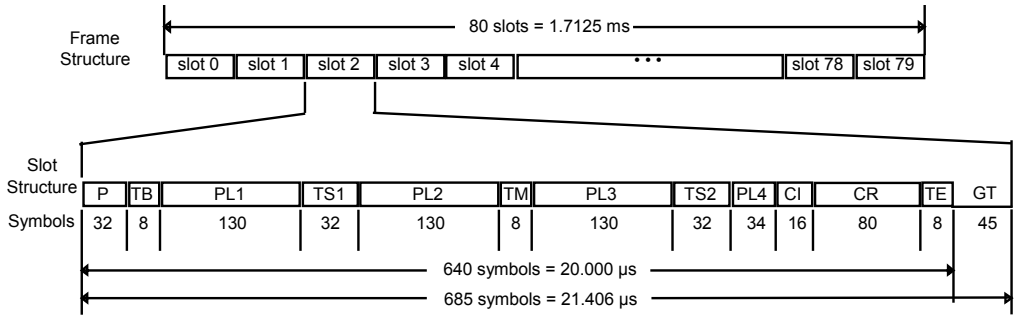

Fig. 1. Slot and frame structure

Multiple access scheme of TDMA is employed to transmit two ATM cells in a burst using offset quadrature phase shift keying (OQPSK) modulation with transmission rate of 32 Mbaud to attain the user bit rate of approximately 34 Mbit/s excluding overhead.

2.2 Functions and Technologies of BBPU

Functions and baseband processing technologies of the BBPU designed are as follows:

- Digital modulation of OQPSK baseband signal mapping
- Equalisation of the received signal based on the Viterbi Algorithm
- Training sequence detection for acquisition of the slot synchronisation and channel impulse estimation.
- Forward error correction using a Reed-Solomon code
- TDMA transmission control of framing/deframing and slot synchronisation

The overall configuration and functions of the BBPU are shown in Fig. 2.

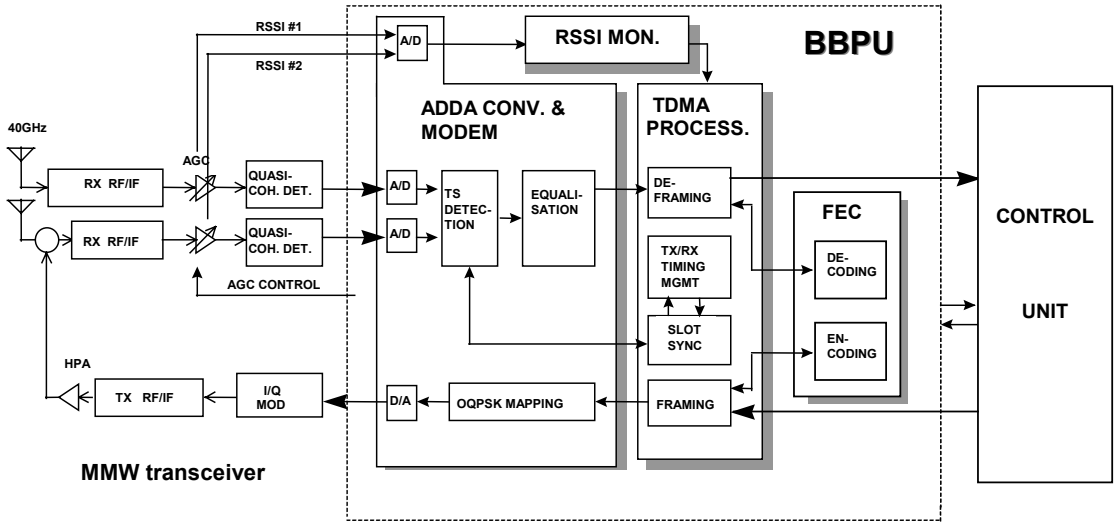

Fig. 2. Configuration and function of the BBPU

2.3 Equalisation Technology

The features of the equaliser in SAMBA are as follows:

1) Decision-Feedback Sequence Estimation (DFSE) with diversity combining is employed;
2) Modulation scheme is a single carrier modulation with offset QPSK (OQPSK).

Regarding the first item 1), the channel model for SAMBA is line-of-sight (LOS) and assumes that maximum delays due to reflections are up to 16 bits. As the number of states for the optimal maximum-likelihood sequence estimation (MLSE) receiver grows exponentially with the channel memory length normalized by bit duration, such MLSE scheme would require for the SAMBA environment 2^{16} (65,536) states, which is practically impossible. Therefore, the equaliser shall employ a state-reduction algorithm like DFSE, which on the other hand implies some performance

degradation compared with MLSE. However, in LOS environments, this degradation due to state-reduction is relatively small. For SAMBA trial platform, employed equalization scheme is 8-state DFSE with diversity combining.

As regards the second item 2), OQPSK has a good spectral efficiency equal to QPSK; indeed its maximum frequency band in baseband is less than half of bit-rate. Moreover, OQPSK with GMSK-like mapping can be treated as narrow-band $\pi/2$ shift BPSK, which enables the Viterbi equaliser to operate at bit-rate and also not to suffer from degradation due to timing offset. The equaliser and the synchronizer in the SAMBA Trial Platform operate as follows:

a) a cross-correlator estimates bit-rate sampling timing and channel impulse response (CIR) for each diversity branch at the same time;

a) DFSE operates based on the estimated timing and CIR, and combines the two branch metrics corresponding to the diversity antenna branches.

2.4 Forward Error Correction

Given a bit error rate of $5x10^{-3}$ with a bursty error pattern at the output of the equaliser, forward error correction (FEC) using Reed-Solomon (RS) codes turns out to be appropriate to protect payload and control information from residual errors after equalization. In accordance with the frame structure as displayed in Fig. 1, a (130,110) RS code over symbols from GF(2^8) has been chosen. This code is capable of correcting up to 10 symbol errors per frame, with each symbol consisting of 8 bits.

3. Design and Implementation of Main Functions

3.1 Development of ASICs

Five kinds of ASICs are newly developed for the BBPU:

- Equalisation ASIC
- Training Sequence Detection ASIC
- Modem Control ASIC
- TRX Control ASIC
- FEC Codec ASIC

Specifications of the developed ASICs are summarized in Table 2. State of the art semiconductor technology has been employed to develop high-density ASIC for high-speed operation; the equaliser ASIC, for example, is developed using 0.35-um CMOS ASIC technology with 250 KGates. The developed ASICs are mounted on two boards of (as shown in Fig. 3.) :

- Modulation/Demodulation Board
- TDMA Processing Board

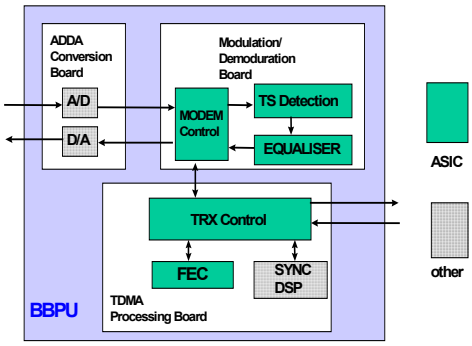

Fig.3 ASICs developed for the BBPU

Table 2. Description of the hardware technology and functions

ASICs	Basic function	Gate volume	Operation speed	Technology (micron)
Equalisation	DFSE + combined with diversity	250 K	16 MHz	0.35 (CMOS Gate array)
TS Detection	TS Detection, CIR Estimation	250 K	32 MHz	0.35 (CMOS Gate array)
Modem Control	OQPSK signal Generation etc.	40 K	64 MHz	0.44 (CMOS Gate array)
TRX Control	Framing/Deframing, Timing Control	56 K	32 MHz	0.44 (CMOS Gate array)
FEC	Reed Solomon Encoding/Decoding	90 K	64 MHz	0.5 (CMOS standard cell)

3.2 A/D-D/A Conversion

The A/D-D/A conversion board is designed to meet the challenging requirement of handling high-speed parallel signals. On the transmit side, the OQPSK signal produced in the Modem Control ASIC is converted into analog signal at the rate of 32 Mbauds.

On the receive side, the received baseband signals in I and Q channels are sampled with asynchronous 64 MHz clock. 8-bit quantization is accomplished to guarantee satisfactory performance of TS detection and equalisation in the environment of multipath fading. In addition, the RSSI signals supplied by the AGC amplifiers are sampled with 8 MHz clock and also converted into 8-bit digital signals.

3.3 Modulation/Demodulation

Functions of modulation and demodulation are accomplished by three ASICs:

- Equalisation ASIC
- TS Detection ASIC
- Modem Control ASIC.

The function of the Equalisation ASIC is to equalise the received signal distortion due to fading and to provide demodulated data; the scheme of the equalisation is DFSE, as described in Section 2.3. The Equalisation ASIC also achieves diversity combining of the signals received in two diversity branches.

The function of the TS Detection ASIC is to correlate the received signal with the stored replica of the training sequence signal, and to acquire the slot synchronisation prior to equalisation. The TS Detection ASIC also has a function of channel impulse response (CIR) estimation for the equalisation.

The function of the Modem Control ASIC is to produce baseband OQPSK signals on the transmit side, and also to manage and control the operation of other ASICs based on the synchronisation information on the receive side.

Design feature of the modulation/demodulation board is that design concept of parallel processing is introduced to mitigate the requirement on the critical operating speed of ASICs; four parallel processing is done with the Equalisation ASICs, each operating at the clock rate of 16 MHz. The modulation/demodulation board thus includes a total of 10 ASICs and 3 PLDs.

3.4 TDMA Processing

Functions of TDMA processing is accomplished by one ASIC and a digital signal processor (DSP):

- TRX control
- TDMA slot synchronisation management

The functions of the TRX control are:

- framing and deframing of transmitted and received data sequence according to the slot structure, respectively
- maintaining the TDMA slot timing
- interface function to the control unit
- interface function to the millimeterwave transceiver unit

The functions of the TDMA slot synchronisation management are:

- management of the slot synchronisation for initial acquisition
- scanning of the received signal strength indication (RSSI) level for a neighborhood cell
- radio handover function

For the purpose of handover, management of TDMA slot synchronisation are done by two counters on the TDMA processing board, thereby enabling to keep slot synchronisation during the period of monitoring a candidate channel in the neighborhood cell and also to realize a fast handover.

Design concept of parallel processing is also employed in designing the TDMA processing board, and the maximum processing clock rate is lowered down to 16 MHz.

3.5 Forward Error Correction

The Reed-Solomon encoder and decoder are implemented on a common, single ASIC using 0.5 micron CMOS standard cell technology.

Symbol-serial data transfer to and from the TRX Control ASIC is carried out at a rate of 8 MHz. With each code symbol consisting of 8 bits in parallel, this results in an effective data rate of 64 Mbit/s. In order to achieve the specified maximum decoder latency of 2 frames [4], eightfold overclocking is employed for the main internal decoder operations, which results in about 40 % of the circuit operating at 64 MHz.
With each frame, the decoder provides a flag whether the frame was correctable or not, thus delivering an indicator for Automatic Repeat Request (ARQ). In the case of correctable frames, the number of symbol and bit errors are also determined by the decoder. This additional information can be used for more detailed link quality measurement.
For board test and performance evaluation purposes, a transparent operating mode is provided in order to bypass the encoding and decoding operations and to transmit frames uncoded. In addition, the chip covers built-in self-test facilities for post-processing and in-system operation tests.

4. Performance evaluation

Bit error rate at the output of the equaliser shall be less than $5x10^{-3}$, as specified in [3]. This section compares BER performance between simulation results and experimental ones. Channels assumed are AWGN channels and the 2-path fading channel shown in Table 3.

Table 3. 2-path fading channel model

no. of taps	relative delay (nsec)	relative power (dB)	Spectrum
1	0.0	0.0	Rice(K=6.0dB)
2	250.0	-6.00	CLASS

Figs. 4 and 5 show BER performance on AWGN channel and the 2-path fading channel, respectively. Experimental data close to the simulation data are obtained.
In addition, degradation caused by nonlinearity of the RF amplifier has been evaluated by computer simulation. Fig.6 compares the BER performance with nonlinear amplifier (limiter) to that with linear amplifier. The channel is assumed as the PDP_100_10 as described in ref [2]. This simulation result shows that the degradation is small, which indicates the robustness of the equalization scheme to the nonlinearity.

Fig. 4. BER performance on AWGN channel

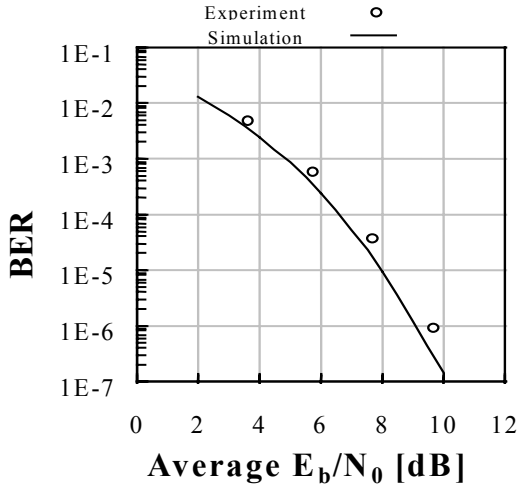

Fig. 4. BER performance on AWGN chnnel

Fig. 5. BER performance on the 2-path fading channel

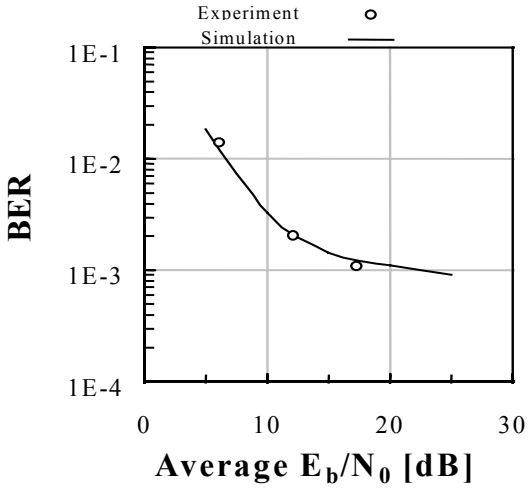

Fig. 5. BER performance on the 2-path fading channel

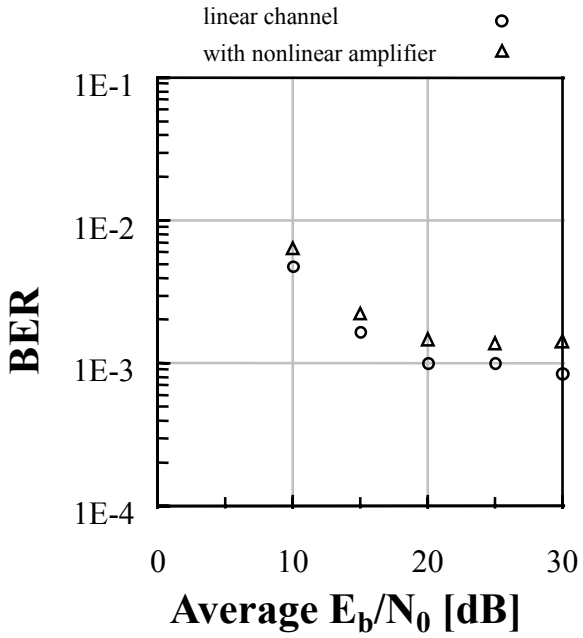

Fig. 6. BER performance with non-linear power amplifier (limiter)

5. Conclusion

A baseband processing unit has been designed and implemented for the SAMBA Trial Platform. The BBPU performs the necessary functions of digital modulation, demodulation with Equalisation, TDMA processing and FEC for broadband digital signal transmission in the environment of high-speed mobile applications. Technologies have been developed including equalisation technology based on DFSE, and several high-density ASICs are newly developed. Performance of the BBPU was evaluated by computer simulation and experiments, and it was confirmed that the BBPU achieves the good BER performance.

References

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