Reconfigurable Radio Case Study: A Software Based Multi-standard Transceiver for UMTS, GSM, EDGE and BlueTooth

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I. Introduction

In a near future, base stations in Europe and Japan will have to support at least the following communication standards: GSM, EDGE, UMTS-FDD and UMTS-TDD, adding BlueTooth for terminals. A software radio (SWR) approach should permit to make substantial savings by avoiding the duplication of the entire radio systems in the equipment. This will be beneficial for both OEMs and network operators and consequently for the final user. SWR consists in taking advantage of the re-configurability properties of properly designed digital systems in order to implement all these different standards with the same components.

In this paper we shall describe a case study of the *Reconfigurable Radio* approach which consists in using a unique hardware platform for the implementation in software of the modulation/demodulation (referred to as modem for brevity) schemes of various standards. The standards under consideration are: GSM/EDGE/UMTS/BlueTooth. Such a choice is very interesting in many aspects. First, it addresses the scenarios of standard transition and operation in multistandard environments. Second, considering all these different modulation schemes (PSK, FSK, constant envelope, frequency hopping etc.) permits to gain a better insight and a global view of the modulation topic in multi-standard equipment.

The rest of the paper is organized as follows. First modulation aspects will be reviewed for a multi-mode GSM/EDGE/UMTS and BlueTooth transceiver. Emphasis will be given on several theoretical aspects which permit to obtain efficient digital implementations. The generic platform used as a proof of concept will be presented, followed by the mapping of the software on the hardware. The last part deals with performance, in terms of signal quality and speed of execution. Finally, some conclusions are drawn regarding the future of the Reconfigurable Radio approach, its deployment applications and challenging topics for future studies.

II. Implementation Aspects And Scope

The same hardware is able to support either GSM, or EDGE, or UMTS, or BlueTooth modulation / demodulation schemes just depending on a configuration file. These are GMSK, 3pi/8 O-QPSK with gaussian pulse shaping, QPSK with RRC pulse shaping and GFSK with Frequency Hopping respectively. Such a wide panel of modulation schemes is considered to demonstrate the universality of the method. The main properties of the studied standards and their impact on the implementation of the modulators and demodulators will be recalled in the final paper.

It should be noted that SWR benefits from technology progress in IF acquisition using under-sampling techniques which is now a reality. Real-time digital processing until some IF is completely affordable with today's processors for all the considered modem cases. The SWR area is now technically open.

A. Hardware platform

In our laboratory an experimentation platform was assembled to study SWR system design, reconfigurability and reconfiguration. This platform, shown in FIG. 1, has a modular hardware architecture making future hardware upgrades possible. A quad TI C6201 DSP processing board interfaces to the analog world through mezzanine cards for A/D, D/A conversion which includes a by-passable digital frequency translation components (down-conversion/up-conversion).

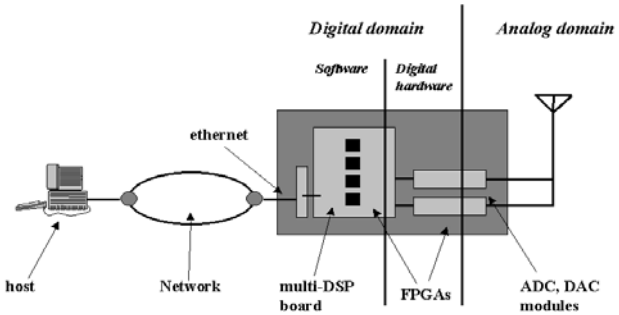

FIG. 1 – Experimentation platform

In the absence of FPGAs, all code development is done in C, to afford a complete portability from this platform to any other processor. The presence of multiple DSPs enables the study of multiprocessing issues. At a second time the introduction of FPGA modules will permit to apply co-design techniques and address hardware and software reconfiguration in a unified manner. Finally, this platform will permit to study the interactions and behavior of the various entities in a cellular network when reconfiguration of the air-interface

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occurs. Experimentation will also give us insight on how reconfigurability needs to be considered for different types of equipment according to the needs and expectations of their respective users (subscribers for terminals and operators for infrastructure equipment). Radio reconfiguration has different facets and is used for different purposes according to the type of equipment.

B. *Employed DSP techniques*

Several DSP techniques are instrumental in obtaining high execution speeds. We take advantage of last technological progress in DAC/ADC design. IF under-samplers have been available on the market for the past few years. Undersampling (bandpass sampling) permits to generate or digitize high frequency signals while processing samples at a much lower rate. A judicious choice of the sampling rate also permits to simplify frequency translation, avoiding the complex multiplication by the carrier in the down-conversion. Moreover, such a choice permits to further reduce the computation complexity of subsequent filtering stages.

In the full paper the software implementation of these digital techniques and others that relate to carrier and symbol timing recovery will be described in detail.

C. *Implementation alternatives*

Our experimentation platform permits to envision different design/implementation approaches each with its own merits. In our case study we explored two such possibilities. Their common point is that both are based on the digital-IF principle. The first uses parametrizable ASIC modules for frequency translation (DUC/DDC); parameters are software controlled and the rest of the processing is implemented in software. The second implementation is a *full-software* one, where frequency translation is also done in software.

III. Experimental Results And Measurements

Performance in terms of quality of the transmitted and received signals, and in terms of the computation speed will be considered for each transceiver chain.

A. *VSA Measurements*

The modulators were validated using a *vector signal analyzer* (VSA). A sample of the results is shown in FIG. 2 for EDGE. Similar results will be given for all the considered modulation standards.

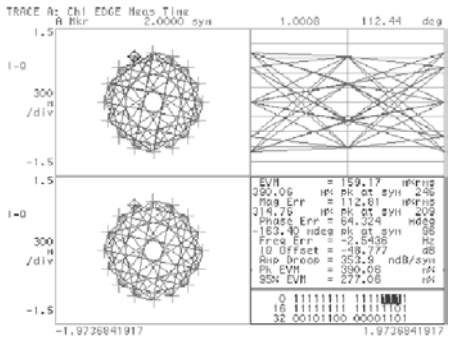

FIG. 2 - EDGE for f_{RF} = 2 MHz

The obtained *Error Vector Magnitude* (EVM) measurements reveal quite satisfactory. EVM is an important metric as far as the implementations of the Tx, Rx chains are concerned.

B. *Implemented performances: Execution speed*

Several performance measurements were obtained. Performance was considered in terms of execution speed (CPU cycle counts) and attained bit rates on one TI C6201 DSP with a 200 MHz clock. The results are given in TAB. 1 for the complete Tx and Rx chains as well as for only the modem functionality. It can be seen that for single processor implementations of Tx or Rx chain, the attained performance is higher than the required for GSM and EDGE. Though this is not the case for UMTS yet, with future releases of the TI C6x taking the CPU clock up to 1 GHz, this will become possible.

Modem	Req. Perf. kbits/s	Tx		Rx	
		Full Tx	Modulator	Full Rx	Demod
UMTS1	3840	1650.7	1921.67	1539.39	1758.24
UMTS2	3840	2264.23	2868.49	2260.29	2870.6
GSM	270.83	397.85	444.6	622.45	753.56
EDGE	812.49	2353.77	3107.95	1329.27	1520.19

TAB. 1 - Attained bit rates (chip rate for UMTS)

Another interesting measurement that will be shown is the number of processor cycles per bit required. Finally, the decomposition of the processing time among the various transceiver functional blocks is a very useful information in order to get a quantitative view of the implementation complexity issues. Results are available for all the standards under consideration. These measurements also give good indications which are the functional blocks to optimize or to implement on reprogrammable hardware (e.g. FPGAs).

IV. Conclusions

In this paper a complete case study for a Reconfigurable Radio design approach will be presented. Software Radio based equipment will become increasingly useful in a multistandard operation environment. The main elements of our approach is the treatment of the GSM/EDGE/UMTS and Bluetooth modem functionality on a common hardware platform based on state-of-the-art VLIW DSPs (TI C6x). In order to obtain good execution speed performances several signal processing techniques were employed like: digital IF, undersampling, digital interpolation/decimation, polyphase filters etc. These useful techniques will be described and their usefulness will become obvious by the performance measurements which will also be presented. It is worth noting that all software development was done in C.

Though our hardware platform is more appropriate for infrastructure equipment due to performance, cost, power and size constraints, the validity of our approach also stands for terminal equipment provided that the involved component technologies will be able to satisfy the terminal design constraints.