

Full Digital IF UMTS Transceiver for Future Software Radio Systems

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Topic Area: . System architectures, aspects and Evaluation

In the future the evolution of mobile communications towards and beyond 3G, will accentuate the need for flexible and evolutionary equipment being able to operate in multi-standard environments. In this context the *Software Radio* approach is a promising way to tackle many of the technical issues arising from requirements for multi-standard operation, adaptability and cost efficiency. However experimentation is now needed in order to better understand and concretely demonstrate how to realize the expected benefits and take advantage of software radio technology. In this paper a software radio modulation/demodulation testbed for UMTS is described with emphasis on both algorithmic and implementation aspects. Two different implementation alternatives are evaluated and their performance as well as system quality aspects are discussed.

***Index Terms*--Software Radio, UMTS, digital IF, soft IF, Digital Signal Processor, undersampling...**

I. INTRODUCTION

MIGRATION From 2G to 3G will necessitate huge investments for infrastructure, all the more so as 3G will not be a unique standard, but a set of standards. As this transition will not be a switch but a long process, there will be a more or less long period of cohabitation between standards of 2G and 3G. The cost will not be only caused by equipment replacement, but also by operation and maintenance that is associated. What about the hardware adaptation to this situation? Will manufacturers simply offer equipment with incremental capabilities but a complete new design at each step?

It is now time to think the equipment design in another way. It is obvious that the processing power needed for 3G will be much greater than for 2G and 2.5G. So a platform able to process a full 3G digital implementation will be also able to support consequently all previous standards. For doing so it is necessary to provide as soon as possible concepts, hardware platforms and IPs for a fully scalable, portable, versatile, universal 3G digital mostly software equipment.

This assessment implies three main points. First, as much as possible of the radio system must be implemented in the

digital domain and if possible in software. Secondly, systems must be designed for reconfigurability to support the re-configuration of both software and hardware based subsystems. Finally, to enable the upgradability and the evolution of the products hardware re-configuration should also include capabilities such as "plug & play" modules.

To increase flexibility it is already common practice to implement in terminals and base stations simple or low speed baseband (BB) digital processing functions of transceivers in software for digital signal processors (DSPs). We propose here to extend the action of DSPs to include also high speed digital baseband functions and even IF processing including frequency conversion.

In this paper it is experimentally demonstrated that this increasingly digital approach is now feasible, even for 3G waveforms as UMTS, with current technology at least for infrastructure equipment. The rest of the paper is organized as follows: after a precise description of our software radio (SWR) platform, the information necessary to make a digital implementation of UMTS modulator and demodulator is given. The scope of this study is restrained to the digital implementation of the modulation and demodulation blocks of a UMTS transceiver, including pulse shaping and frequency conversion between BB and IF. Next, two different mappings of the functional blocks on the hardware platform are explored; a full software and a mixed software and ASIC solution. Finally, the last part deals with performance, in terms of signal quality and speed of execution on the DSPs.

II. A SWR EXPERIMENTATION PLATFORM

In our laboratory an experimentation platform was assembled to study SWR issues relating to system design, reconfigurability and reconfiguration. Such experimentation will give us insight on the technical issues raised when the SWR concept is applied to mobile communications equipment. It will also give us insight on how reconfigurability needs to be customized for different types of equipment according to the needs and expectations of their respective users (i.e. subscribers for terminals and operators for infrastructure equipment).

A. General description

The core of our SWR platform is multi-DSP board based on last generation VLIW processors (four TI C6201 at 200 MHz). It has a modular hardware architecture making future upgrades possible. The presence of multiple DSPs enables the study of multiprocessing issues. At a second time the intro-

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duction of FPGA based modules will permit to apply co-design techniques and address hardware and software reconfiguration in a unified manner [1]. Finally, this platform permits to study the interactions and behavior of the various entities in a cellular network when reconfiguration of the air-interface occurs. Currently, in the absence of FPGAs, all code development is done in C, enabling portability from this platform to any other processor, as the SWR dogma requires. The price for portability is a limitation on execution speed, depending on the quality of the associated software tools (i.e. the C compiler).

The interface of this board with the analog world is via wideband transmitter (Tx) and receiver (Rx) modules based on wideband D/A and A/D components. Module parameters are fully software controlled and their principle of operation is described next.

B. Detailed Tx

The physical architecture of the transmit part of our platform is depicted in FIG. 1. The DSP processing board interfaces to the analog world through a mezzanine card of digital to analog conversion which includes a by-passable *digital up-converter* (DUC) for frequency translation from baseband to some carrier frequency¹. Frequency translation can be done digitally by multiplication of the I and Q data stream by digitally generated (sampled) cosine and sine waves of the programmed carrier frequency (DDS: Direct Digital Synthesis) as shown on FIG. 1. The sampling frequency is a software controlled parameter.

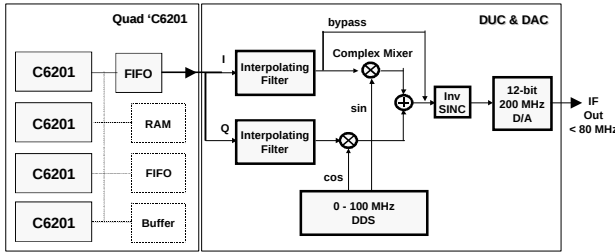


FIG. 1 – Platform transmitter module (Tx)

This hardware structure which is appropriate to implement the functionality of a digital transmitter depicted in FIG. 2.

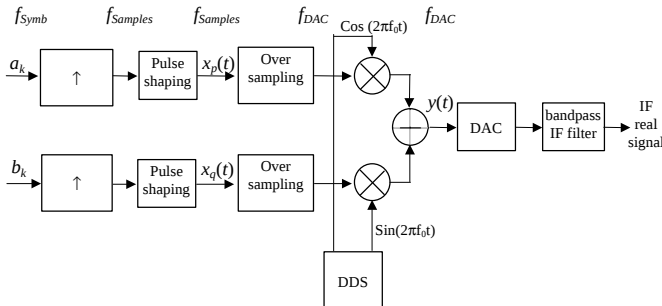


FIG. 2 – Functional diagram of the digital transmitter

SWR techniques aim at performing as much as possible

processing in digital and particularly in software by moving the digital to analog conversion (DAC) as close as possible to the antenna. As already mentioned, the goal is to produce a sampled version of the modulated signal by using a sampling rate f_{DAC} greater than $2f_0$, where f_0 is a low carrier frequency. Taking advantage of the replicas of the digital signal the real carrier frequency f_{RF} is chosen at $n.f_{DAC} + f_0$ where n is a positive integer.

C. Detailed Rx

Similarly, the Rx part has the structure depicted in FIG. 3. The principle for processing and acquisition is the same as for the transmitter. The digital down converter is *by-passable* to allow a *full software* implementation of the down-conversion in the DSPs.

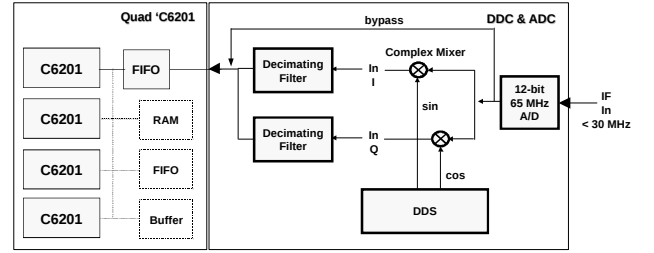


FIG. 3 – Platform receiver

For a SWR receiver, ADC conversion has to get as close to the antenna as possible. Thus, to adhere to the SWR design philosophy, a wideband RF sampling ADC replaces the multiple front ends [2]. A top-level functional block diagram of such a digital receiver is shown in FIG. 4. Briefly, the digital Rx approach consists in sampling the signal after filtering by an analog anti-aliasing filter, shifting to zero the center of the band of interest by the quadrature modulator. The signal is usually filtered to reduce noise, and/or ISI and to suppress spectral images. Decimation then produces a signal at a sample rate commensurate with its bandwidth, followed by a set of other baseband processing operations (synchronization...) to obtain the information bit stream.

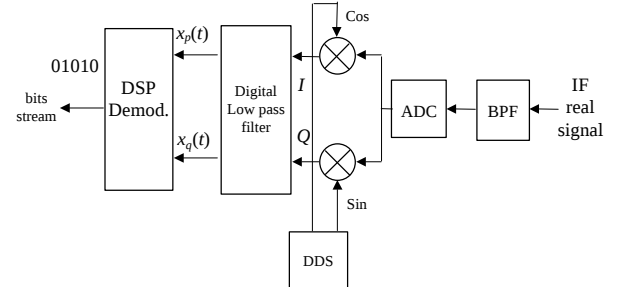


FIG. 4 – Functional diagram of the digital transmitter

III. DIGITAL UMTS MODULATION

SWR requires to think the design of a radio system in a completely new way. That is why it is so important to revisit some of the basic theoretical aspects. Furthermore the digital signal processing implementation, SWR is associated with, also permits in some cases to greatly simplify the operations of the transceiver.

¹ Note that the DDS function may be realized either by the DUC or by software in the DSP.

The main idea is that the same architecture has to be used for the different radio systems. Taking advantage of the universal decomposition of any radio signal in its quadrature components, a complex representation of the baseband signals is implemented [3].

Let's now describe into some detail the modulation and pulse shaping functions of the UMTS standard [4] which is the topic of our case study.

A. Direct sequence spread spectrum

3GPP chose direct sequence spread spectrum techniques (DSSS) for three major reasons. First, it is a good candidate as an efficient multiple access method that permits to increase the capacity in a cell: CDMA. The main advantage is to have a fluctuating limit for saturation. Note that code *orthogonality* must be particularly studied. Second, as mobile phones evolve in a multipath environment, it is possible to benefit from the properties of multipath processing offered by DSSS: for which RAKE receivers seem to be unanimous. Note that their performance directly depend on the processing gain and the chip rate (delay resolution). Finally, another way of increasing the capacity is to minimize the interference between neighbor cells thanks to the low power density level occupied by a DSSS signal. The major drawback of DSSS CDMA, the near-far effect, is solved with power control techniques. Note that 3GPP proposes an evolutionary standard with many digital processing techniques that may be added in the medium term (sectorization, Tx diversity, smart antennas, multi-user detection...)

B. UMTS modulation

The chosen modulation for UMTS is based on QPSK, whose quadrature decomposition is the following:

$$x_p(t) = \sum_k a_k g(t - kT_s), \quad x_q(t) = \sum_k b_k g(t - kT_s)$$

where:

- a_k, b_k represents symbols stemming from mapping,
- $g(t)$ represents the impulse response of the pulse shaping filter,
- T_s represents the symbol duration.

According to the specification of W-CDMA, a *root raised cosine* filter with a *roll-off* factor of $\alpha = 0.22$ is used for pulse shaping. Its impulse response is:

$$g(t) = \frac{4a}{p} \times \frac{\cos\left(\frac{pt}{T_s}(1+a)\right) + \frac{\sin\left(\frac{pt}{T_s}(1-a)\right)}{\frac{pt}{T_s}}}{1 - \left(\frac{4at}{T_s}\right)^2}$$

This pulse shaping is a global Nyquist filtering distributed between the transmitter and the receiver, suppressing that way the inter symbol interference on the complete system chain.

C. Digital IF

We do not only demonstrate here that it is possible to process non-zero frequency signal in real-time and it also allows

simplifications on usual baseband digital processing functions too. Indeed, far away from decreasing the speed performances, digital up/down-conversion accelerates the computation as shown in paragraph III.E.

We implement here a digitization at the IF level. This is only due to the technological constraints of our platform. The very same processing is applicable to the RF signal. We just have to wait for the technology to be available at lower prices and for the required quality.

Down-conversion from RF to IF can be performed by a usual multiplication by a sinusoid. It has not been implemented in our testbed at this stage of our development. The radio signal is transmitted at IF (carrier around few MHz).

The transmitted signal is translated here from baseband to a certain carrier frequency (that we'll call IF), and converted from complex to real in the digital domain. At the receiver, we have to digitize a real IF signal, to downconvert it to baseband, and extract its complex components in the digital domain.

This kind of computation is very well suited to current digital signal processors (DSP) architectures. This requires to master theoretical aspects of the problem and to use few mathematical simplifications.

Other advantages in comparison to analog complex mixer, are the quality of the generated signal since all imperfections of the analog components are avoided. And if we consider that the whole conventional heterodyne structure can be integrated in a DSP, form factors, costs and power consumption problems are minimized when in digital.

Last but not the least, digital IF permits to benefit from the sampling replicas and to increase that way the frequency shift for up or down-conversion. In other words, it is possible to generate high frequency replicas at Tx while processing at lower rates. At Rx undersampling techniques enable to obtain low frequency replicas while digitizing high frequency signals. Then a low speed computation is only required to complete the complex mixing for down-conversion to baseband.

D. Undersampling

We take advantage of last technological progress in DAC/ADC design. "IF under-samplers" [7] or "IF sampling ADC" [8] have been available on the market for the past few years. Their particularity consists in having a much greater analog input bandwidth than half of their maximum sampling rate. In consequence, it is possible to digitize analog band-limited signals at sampling rates less than twice the maximum frequency contained in the signals, but at least twice its bandwidth. This is under-sampling. Carrier modulated signals of FIG. 5 lie in this category.

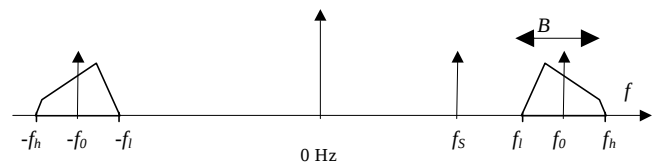


FIG. 5 – Spectrum of band-limited signal (f_l : low frequency, f_h : high frequency)

In such cases two conditions need to be satisfied in order to

be able to successfully reconstruct the sampled signal:

- sample at a rate which is at least twice the bandwidth of the signal.

$$f_s \geq 2(f_h - f_l)$$
- the band of interest should not lie on integer multiples of half the f_s

$$\frac{2f_h}{k} \leq f_s \leq \frac{2f_l}{k-1} \quad \text{with} \quad 2 \leq k \leq \frac{f_h}{f_h - f_l}, k \in \mathbb{N}$$

With this condition spectrum overlap of the signal replicas is avoided. This is called under-sampling, bandpass sampling, harmonic sampling, Super-Nyquist sampling. This last condition clearly says that even if the first condition is respected not all sampling frequencies are allowed when under-sampling is considered. FIG. 6 (taken from [9]) gives allowed and forbidden (gray) regions for the sampling frequency versus the band of interest position.

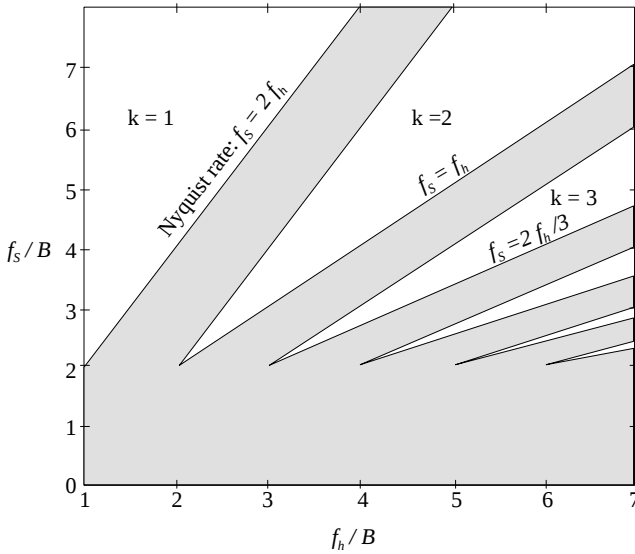


FIG. 6 – Allowed sampling rate in respect to band position

Analogists will answer that even if ADC and DAC could reach the adequate properties, computing strength is far from permitting to process the sample rates generated by the digitization of RF signals. Tricks may be applied there too.

It is effectively possible to generate or digitize high frequency signals while making calculations at a much lower rate. This is under-sampling consequence. The price to pay concerns signal to noise ratio.

E. Under-sampling and digital IF

A very simple realization, which avoids the complex multiplication by the carrier in the down-conversion, can be obtained if we sample the signal according to the equation:

$$f_s = \frac{f_0}{l \pm \frac{1}{4}} \quad \text{for a positive integer } l$$

As an example we take the sign (+) and the relation becomes:

$$e^{-jn2\omega_0 T_s} = e^{-jn4p \left(l + \frac{1}{4} \right)} = e^{-jn4pl} = (-1)^n$$

Substituting this result into the equation related to the

down-conversion process yields:

$$x[n]e^{-jn2p \frac{f_0}{f_s}} = x[n](-1)^n = \frac{\sqrt{2}}{2} [x_{bb}[n] + x_{bb}^*[n](-1)^n]$$

At even sampling instants, $2nT_s$, we obtain the real component of x_{bb} (the imaginary part being equal to zero) and at the odd instants $(2n+1)T_s$ we obtain the quadrature component (the real part being equal to zero).

$$x[n]e^{-jn2p \frac{f_0}{f_s}} = \begin{cases} \sqrt{2} \text{Re}\{x_{bb}[n]\} & \text{for } n \text{ even} \\ j\sqrt{2} \text{Im}\{x_{bb}[n]\} & \text{for } n \text{ odd} \end{cases}$$

As only one sample over two will be conserved after the sample rate decimation, (for example samples related to the sampling instants $2n$) the simplifications of FIG. 7 can be applied.

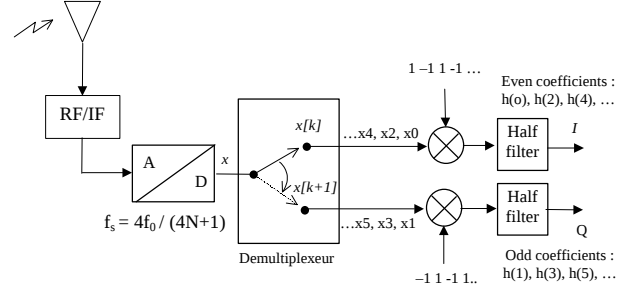


FIG. 7 – Efficient under-sampling demodulator with simplified matched filter

This solution permits to avoid using complex multiplication operations and reduce computation complexity of the filtering operation by half. We will see later in this paper that filtering is the more time consuming operation for the DSP. The benefit of the digital up/down-conversion is increased that much. The same principles may be applied at Tx.

IV. SW IMPLEMENTATION

At a first time our choice is to evaluate current generation DSP processors for the 3G computation load. That is why no FPGA is involved at the moment. Thanks to the scalability and modularity of our platform, we confronted two different digital designs for the UMTS case including digital IF processing. The first solution tries to use most of the available hardware resources of the platform. BB digital processing is performed on the DSP and the frequency conversion is done by the DUC at Tx and DDC at Rx. We call this implementation: hybrid (UMTS-H). Undersampling techniques are involved here. The second implementation alternative gets closer to the SWR concept; all digital signal processing until IF (including frequency conversion) is realized by DSP software. We call this implementation: full soft (UMTS-FS).

A. Methodology

Defining a methodology was a central point in our development approach. The objective of a methodology is to define a coherent and consistent path from a set of requirements to a functionally correct, real-time (R/T) low-level implementation on a given architecture. Any methodology has two main aspects. The first is the definition of a process consisting of a set of activities/tasks that have to be performed in a specified

order. The second aspect is the use of a set of tools to assist the designer in performing the process activities. The adopted development process proceeds by refinement and iteration. Functional, architecture and performance aspects are treated separately to make the problem more manageable. Note that correctness is considered at two levels: functional and temporal.

It is clear that SWR needs to be viewed from a *system-level* design perspective where the radio functionality is just a part of a system and the whole system design has to be addressed within a unified and coherent system development framework. Clearly the complete system design of SWR-based telecommunication equipment is a hardware/software co-design problem [1] since such systems are an assembly of heterogeneous subsystems with either specific or programmable functionality.

B. A hybrid DSP/ASIC implementation: UMTS-H

The functional diagram is the one of FIG. 8, except the inversion of the interpolation and up-conversion blocks at Tx (included in the DUC), and the inversion of the decimation and down-conversion blocks at Rx (included in the DDC). Detailed characteristics are given in TAB. 1.

Tx	Rx
$f_{\text{chips}} = 1 \text{ Mcips/s}$	
$f_{\text{complex chips}} = 500 \text{ ksymbols/s}$	
baseband oversampling (N) = 2	
$f_{\text{samples}} = 1 \text{ Msamples/s}$	
interpolation = 8	decimation = 8
$f_0 = 2 \text{ MHz}$	IF = 10 MHz
$f_{\text{DAC}} = 8 \text{ MHz}$	$f_{\text{ADC}} = 8 \text{ MHz}$

TAB. 1 - Characteristics of the hybrid chain

Undersampling techniques are involved in this method. For demonstration purposes, the 10 MHz replica of the original 2 MHz signal is analog filtered for transmission. Note that we could have chosen any other replica at higher frequencies. This bandpass signal at 10 MHz is generated thanks to a DAC at 8 MHz and at Rx it is digitized by the ADC at a rate of 8 MHz. This effectively is undersampling.

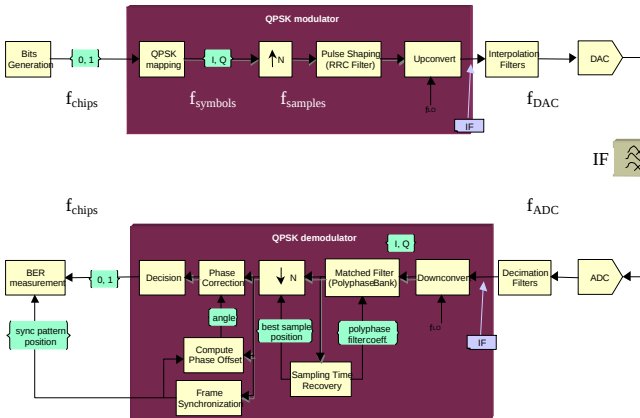


FIG. 8 – UMTS full-soft transceiver

C. A full software implementation: UMTS-FH

The frequency translation of the DUC and the DDC are bypassed². The shadowed areas of FIG. 8 are entirely executed in a DSP that provides an IF signal to the interpolation filter of the DUC and then the DAC at Tx, and directly processes an IF signal from the ADC and the decimation filter of the DDC at Rx.

We will see in next section that even with an oversampling factor of four in the full software approach, as indicated in TAB. 2, it is possible to reach an execution speed higher than the hybrid method with an oversampling of two.

Tx	Rx
$f_{\text{chips}} = 2 \text{ Mcips/s}$	
$f_{\text{complex chips}} = 1 \text{ Msymbols/s}$	
baseband oversampling = 4	
$f_{\text{samples}} = 4 \text{ Msamples/s}$	
interpolation = 16	decimation = 2
$f_0 = 1 \text{ MHz}$	IF = 1 MHz
$f_{\text{DAC}} = 64 \text{ MHz}$	$f_{\text{ADC}} = 8 \text{ MHz}$

TAB. 2 - Characteristics of the full soft chain

In both implementations an all digital mechanism of carrier and symbol timing recovery was adopted. This mechanism based on polyphase filtering will not be detailed here. Thanks to the use of polyphase filters an oversampling factor of 2 gives satisfactory results and has also the advantage of keeping the computational load low.

V. PERFORMANCES

Performance in terms of both quality of the transmitted signal, and of computation speed is considered here. Both UMTS modulator/demodulator implementations were considered. UMTS-FS and UMTS-H denote the full software and the software/ASIC implementations respectively.

A. Measured quality with a VSA

The modulators were validated using a vector signal analyzer (VSA). The results shown in FIG. 9 and 10.

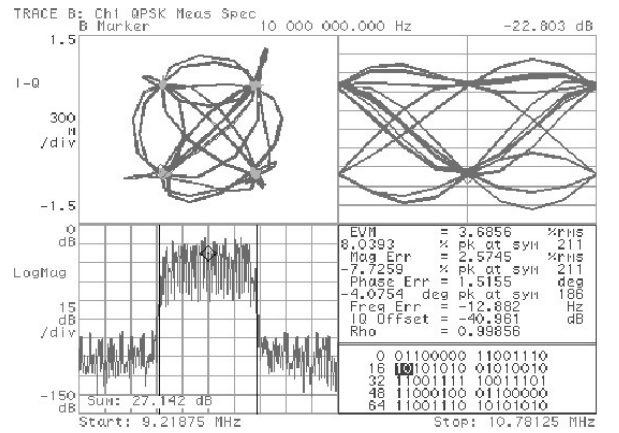


FIG. 9 - UMTS hybrid for $f_{\text{RF}} = 10 \text{ MHz}$

² due to the design of DUC, DDC it is not possible to avoid the interpolation and decimation stages of these components which are not really needed.

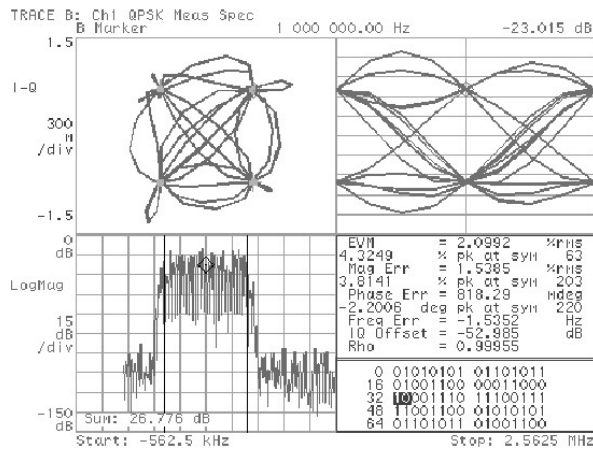


FIG. 10 - UMTS full soft for $f_{RF} = 1$ MHz

Error Vector Magnitude (EVM) figures, UMTS-H: 3.68 %rms and UMTS-FS: 2.09 %rms, reveal quite satisfactory. EVM gives the deviation of a received constellation from an ideal reference constellation. If we assume an optimal receiver EVM provides an indication of whether the transmitter does a good job. Similarly assuming a correct transmitter EVM is an indication whether the receiver does also a good job.

B. Implemented performances

Several performance measurements were obtained. Performance here is considered in terms of execution speed (CPU cycle counts) and attained bit rates on a single TI C6201 DSP at 200 MHz. The results are given in TAB. 3. For the all implementation schemes, we measured the global performance of the Tx, Rx chains as well as the performance of only the modem functionality. Implementation parameters to be taken into account are those of paragraph IV. The Tx full chain consists of: *Bit Generation - Modulator - IO Data Transfer*. Similarly for Rx, the full chain consists of: *IO Data Transfer - Demodulator - Synchronizations - BER*.

Modem	Re-quired Perf. in kbits/s	Tx		Rx	
		Full Chain	Modulator	Full Chain	Demodulator
UMTS H	3840	1650.7	1921.67	1539.39	1758.24
UMTS FS	3840	2264.23	2868.49	2260.29	2870.6

TAB. 3 - Attained chip rates

Note in TAB. 3 that *modulator* represents the symbol mapping and pulse shaping whereas *full chain* at Tx also includes the bit generation and IO data transfers. Up-conversion is comprised in the *modulator* in the case of full soft UMTS. Idem at Tx, *demodulator* contains (down-conversion for UMTS full soft) the matched filtering operation, to which are added decimation, synchronization, BER and IO data transfer for *full chain*.

It can be seen that for single processor implementations (C6201 DSP at 200 MHz) of Tx, Rx for UMTS the attained

performance is lower than the required. However the next release of TI C6x, the C6203 at 300 MHz, will permit single DSP implementations of the modulator and the demodulator to run in real-time. Moreover, the C6x roadmap shows that soon processors at 1GHz clock speeds will be available (i.e. C64x). Having the software written in high-level language code will permit to easily take advantage of technological progress in processor design and manufacturing.

The present measurements indicate that a single C6x could handle both Tx and Rx at the same time and deliver real-time performance. However it must be noted that currently the C6x DSP chip is not destined to mobile terminals due to its high power consumption, size and price.

C. Distribution of the computation load

Another set of measurements investigates how processing time is distributed among the transceiver functional blocks. These measurements give good indications which are the functional blocks to optimize or to implement on reprogrammable hardware (i.e. FPGAs). In the following figures the processing time decomposition as a % of function cycle count over total cycle count, is given. For both implementations full Tx, Rx chains to including data transfer overheads³ are presented and the demodulator part which is a lot more complex than the modulator is considered in detail.

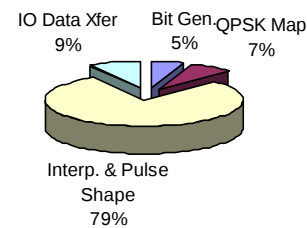


FIG. 11 – UMTS-H processing time decomposition - Tx

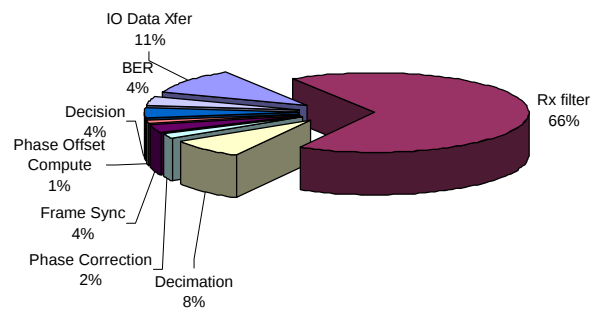


FIG. 12 – UMTS-H processing time decomposition - Rx

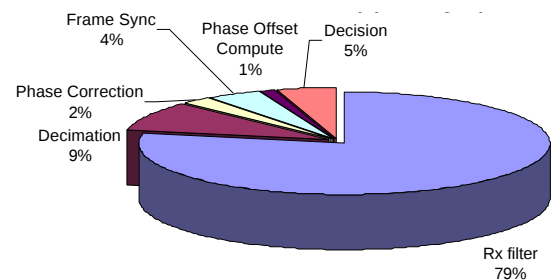


FIG. 13 – Processing time of UMTS-H demodulator

³ this overhead can be masked by employing the DMA channels of the TI C6x that permit to perform data transfer and computation in parallel

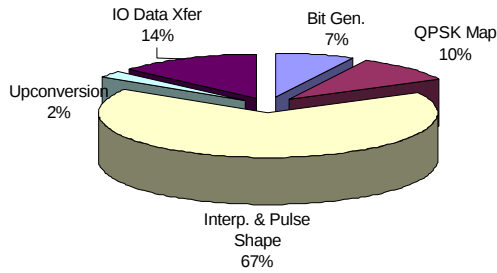


FIG. 14 – UMTS-FS processing time decomposition - Tx

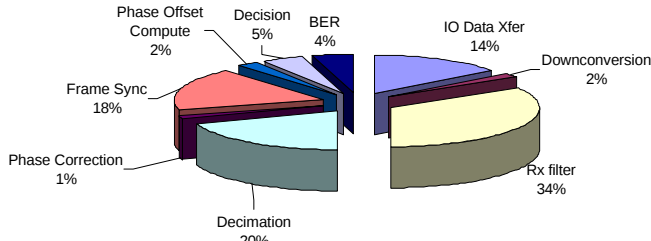


FIG. 15 – UMTS-FS processing time decomposition - Rx

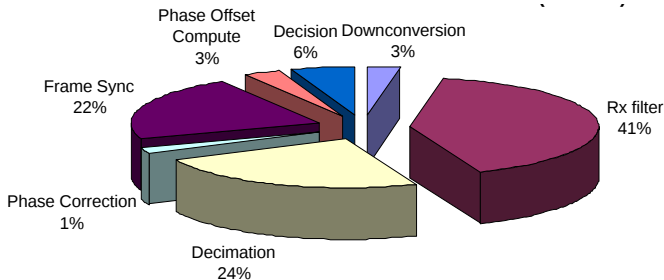


FIG. 16 – Processing time of UMTS-FS demodulator

These results confirm synchronization functions represent almost half of the complexity of the demodulator. It is interesting to notice that in the full software case the computation burden for frequency translation (up-conversion, down-conversion) is negligible thanks to the digital techniques that permit to obtain highly optimized solutions for these functions. Finally, it is clear that filtering for pulse shaping though a simple operation is the most time consuming and this gets worse for higher oversampling factors. Such simple (regular) but time consuming processing is a good candidate for a more hardware oriented implementation. FPGA implementation is very promising in order to retain the flexibility offered by reprogrammability however the system architecture will become more heterogeneous and the development methodologies will need to help the designers cope with this.

VI. CONCLUSIONS

In this paper it was presented how the software radio concept was effectively used to build a UMTS modulator-demodulator. It is evident that several well established but not widely used techniques like undersampling help in making current DSP processor technology deliver the required performance. Taking benefit from technology progress, IF acquisition using under-sampling techniques is now a reality. Real-time processing until IF is completely affordable with today's generations of processors for all these cases. The SWR area is now technically open. Initially SWR technology will find its

way as a mainstream practice in infrastructure equipment and eventually in mobile terminals.

Note that the same hardware has also been successfully used to implement GSM, EDGE, Bluetooth modulation-demodulation schemes. This clearly validates the various advantages of using SWR for multi-standard operation.

Several areas are still open, flexible RF sections, design for reconfigurability, reconfiguration mechanisms, the impact of air-interface reconfiguration on the network etc. As experimentation and further study continue better insight to all those issues will be gained.

VII. ACKNOWLEDGMENTS

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