Reconfigurable Software Radios: a case study for over-the-air bug fixing

proof of concept by lab experimentation

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Outline

- **Introduction & motivation**
- **The result**
  - over-the-air bug fixing demonstration
- **How this result was obtained**
  - key issues
  - technical details
- **Perspectives**
- **Conclusions**

Mitsubishi Electric Telecom

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Software Radio (SWR) Department

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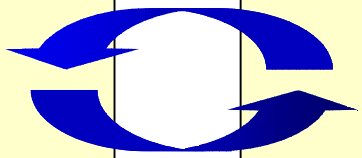
...establishing links between research and applications

Business Units

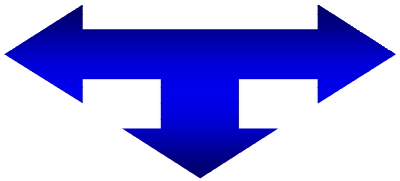
Infrastructure
PDC, PHS and future systems
Mobile terminals
GSM/GPRS, PDC, i-mode, Foma (3G) and future systems



Corporate R&D

Japanese Labs
US Labs
Information Technology Europe (ITE)
VIL: Video and broadcast (UK)
TCL: Telecoms (France)

Huge internal R&D effort on future wireless technologies



Software Radio (SWR)

SWR offers unique opportunities for connecting research to products

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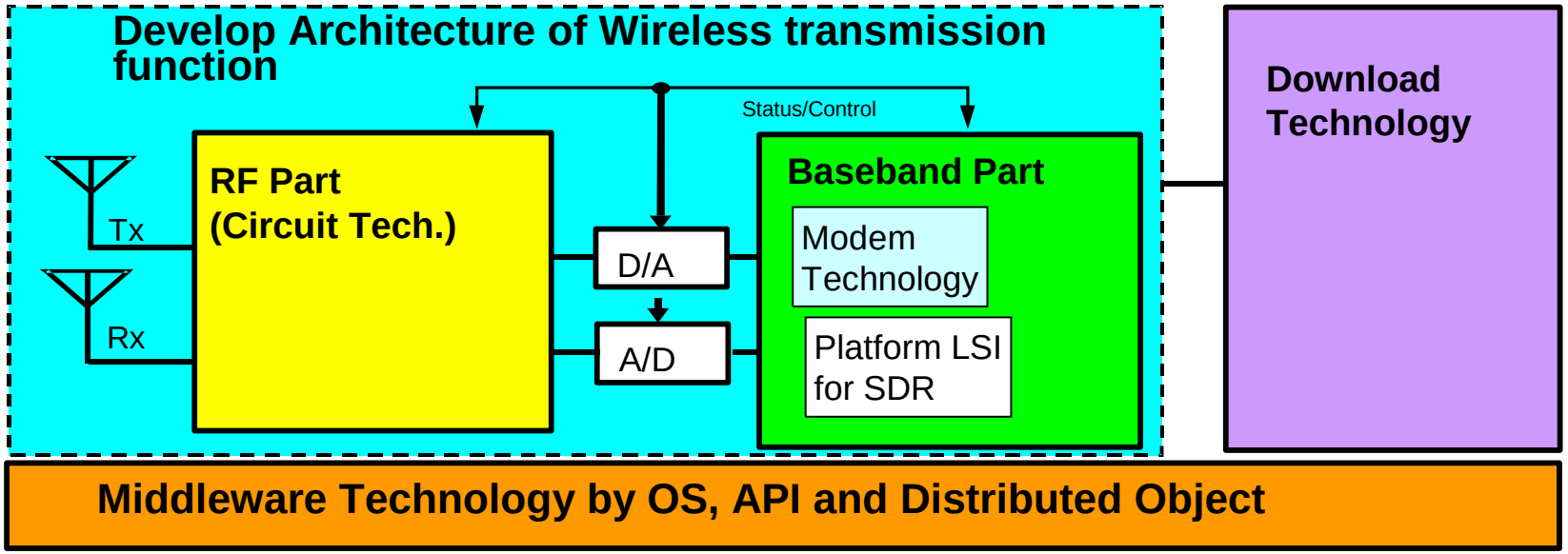
…SWR related activities

- **Mitsubishi is committed to SWR research with activities both in Europe and Japan**
- **Europe**
  - internal research by the ITE SWR department (started 1999)
  - A3S: French national product (RNRT) led by Thales
  - E2R: EU funded integrated project led by Motorola
- **Japan**
  - TAO SDR: Japanese national project led by Mitsubishi

TAO-SDR in Japan

- **Japan National Project**
  - partners: Mitsubishi Electric (leader), Toshiba, Fujitsu
  - duration: 4 years project (02 to 05)
- **Objectives: R&D realization of 4G terminals with key SDR technologies**
  - system architecture and devices for multi-mode/multi-band SDR terminal which supports 100Mb/s transmission rates and realizes seamless connection for multiple wireless systems



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Software Radio and motivations

- **A simplistic view of Software Radio**
  - design as much as possible of a radio system in digital and if possible in software
- **A new way to design radio systems (terminals and BTS)**
  - economic in the long term
    - unique HW platform for several products, shorter design time (more SW design)
    - flexibility (last minute adaptation)
  - easier to manage after selling: updates, bug fixing
- **A solution to multi-standard**

Market data & short-term expectations

- **SDR Forum market survey by Gartner Consulting (jan. 2002) for both US and EU wireless operators:**
  - "SDR technology will have a great benefit in fixing bugs in handset"
  - "rapid SW bug fixing is expected to be a key value proposition for the handset market, especially as 3G emerges"
  - "bug fixing is the clear top choice driven by the need to smooth the introduction of 2.5/3G services"
- **Operators will soon require dynamic reconfiguration for bug fixing**
  - Orange introduced in Oct. 2002 an Over-The-Air phone settings configuration (through SMS): "MyPhoneSettings" (from Swapcom)
    - 20.000 profiles are downloaded every day
    - Orange customer service that answers parameter settings issues saves 180.000 Euros/month

concentrating on short-term applications of reconfiguration today i.e. bug fixing will permit to justify and further develop longer-term applications requiring more investment and effort

Reconfiguration of the physical layer

current status and future needs

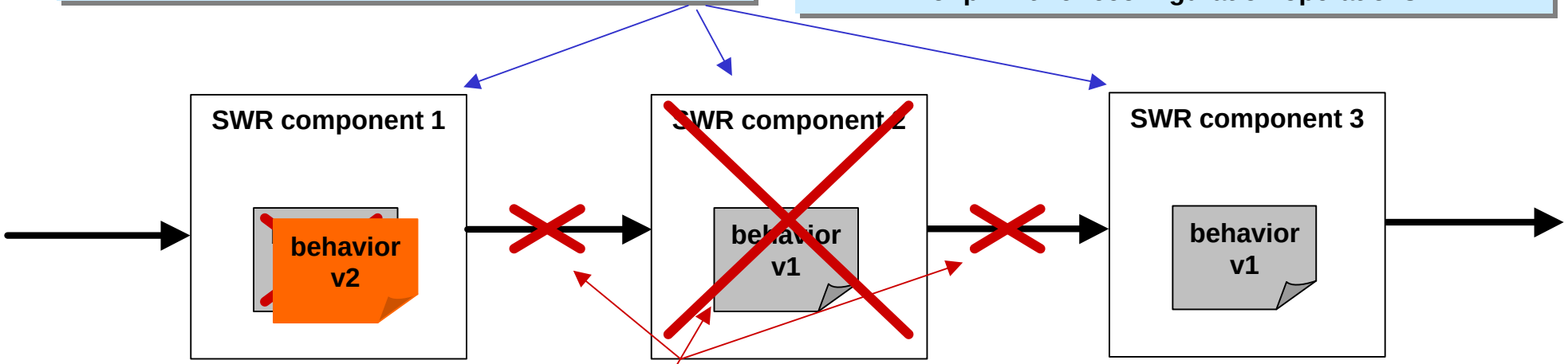
- **Currently some degree of flexibility through adaptation of pre-defined system parameters or functions**
  - physical layer
    - e.g. power control loops, GSM frequency hopping, adaptive equalization
- **More flexibility will be needed in the future**
  - ranging from simple algorithm changes/upgrades to communication standard switch
  - it may influence entities throughout the protocol stack
  - it may happen off-line or on-line (at run-time) and it has to be transparent for the user
- **Requirements**
  - equipment support (mechanisms), network support (signaling, policies)

Reconfiguration of the physical layer

changing structure and behavior

A Reconfigurable Physical Layer system is a collection of interconnected Reconfigurable Physical Layer Functional Blocks

Reconfiguration is the process of manipulation of both structure and behavior in order from an initial configuration to derive a final one through a succession of primitive reconfiguration operations



Simple reconfiguration
change component behavior (algorithm change)
bug fixing
performance enhancement

remove a component

Structural changes (remove/insert components)
on-the-fly re-design of the transceiver chain
better matching the transmission environment

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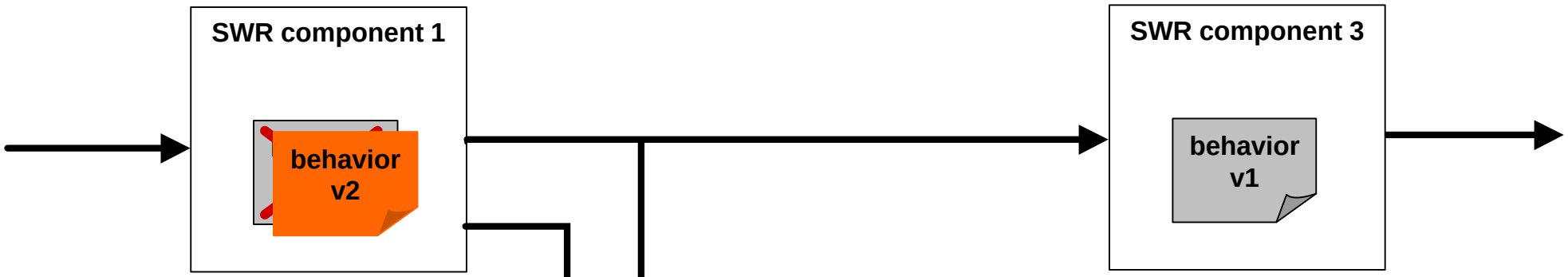

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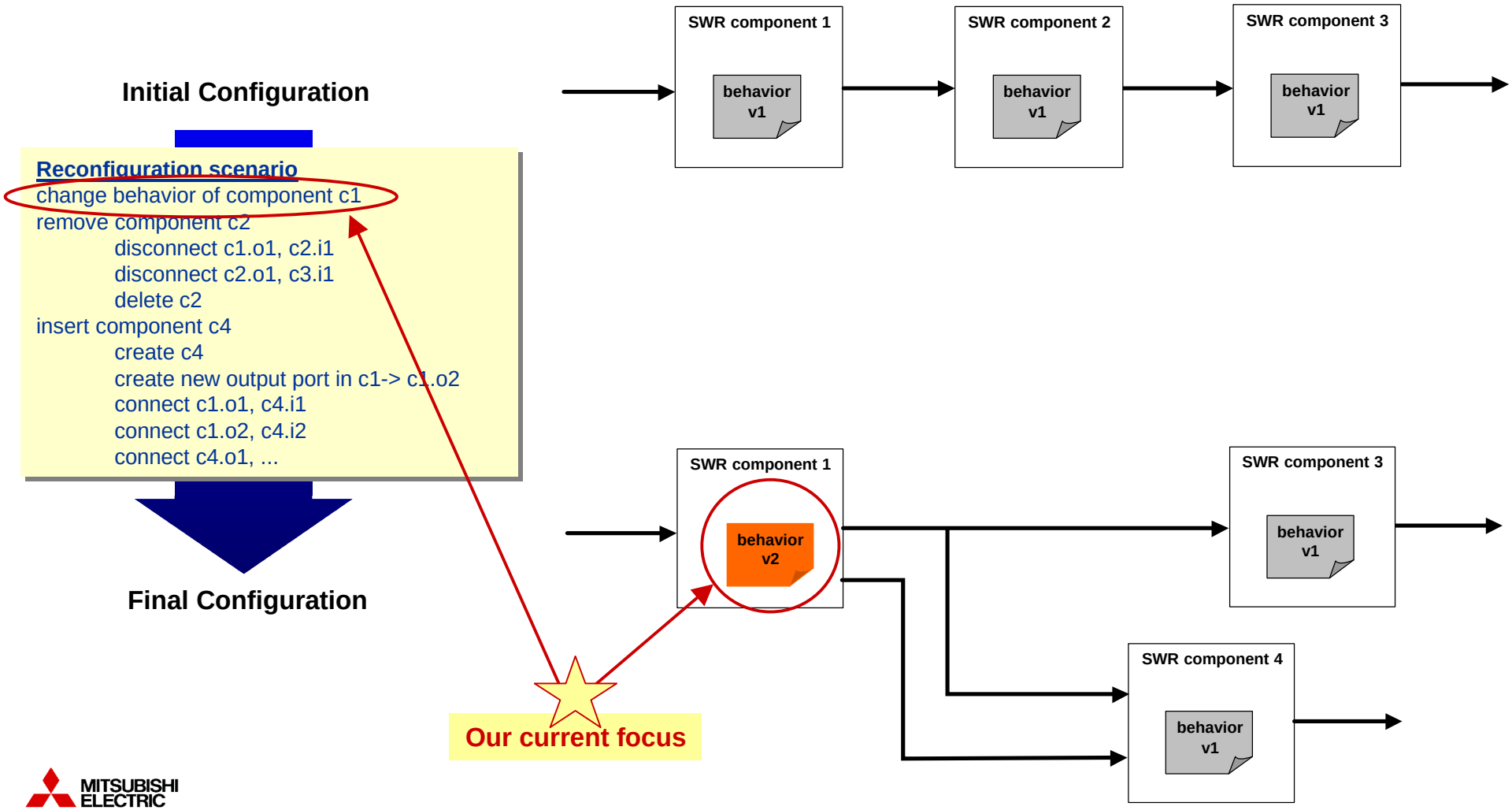
Reconfiguration "script"



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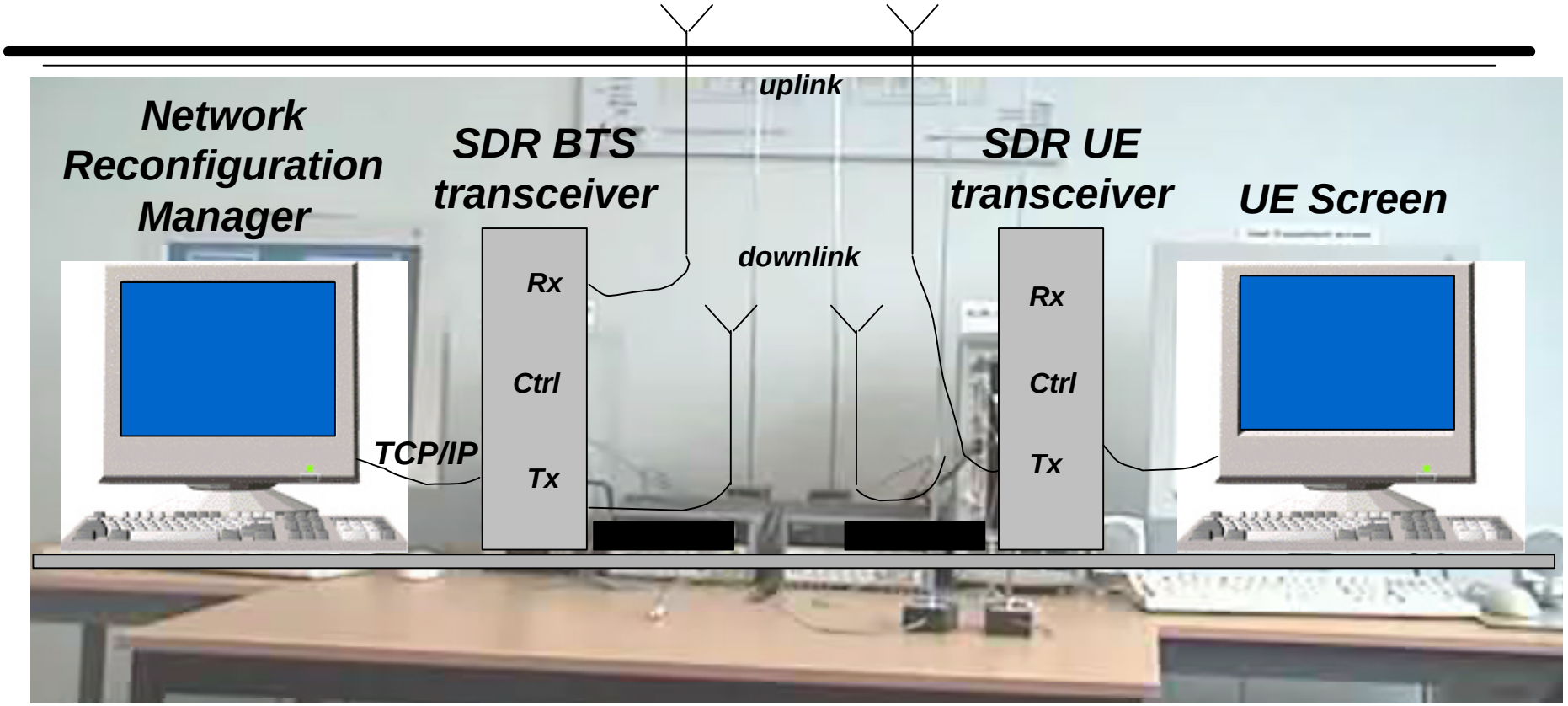
Case study: dynamic reconfiguration

- **SW architecture appropriate for:**
  - heterogeneous systems
    - processors, FPGAs & parameterizable ASICs
  - any functionality
    - physical layer & higher layers
- **tested at the moment**
  - on multi-DSP architecture
  - on physical layer algorithms
  - without structural changes
  - code and/or parameter download

Demonstrator topology

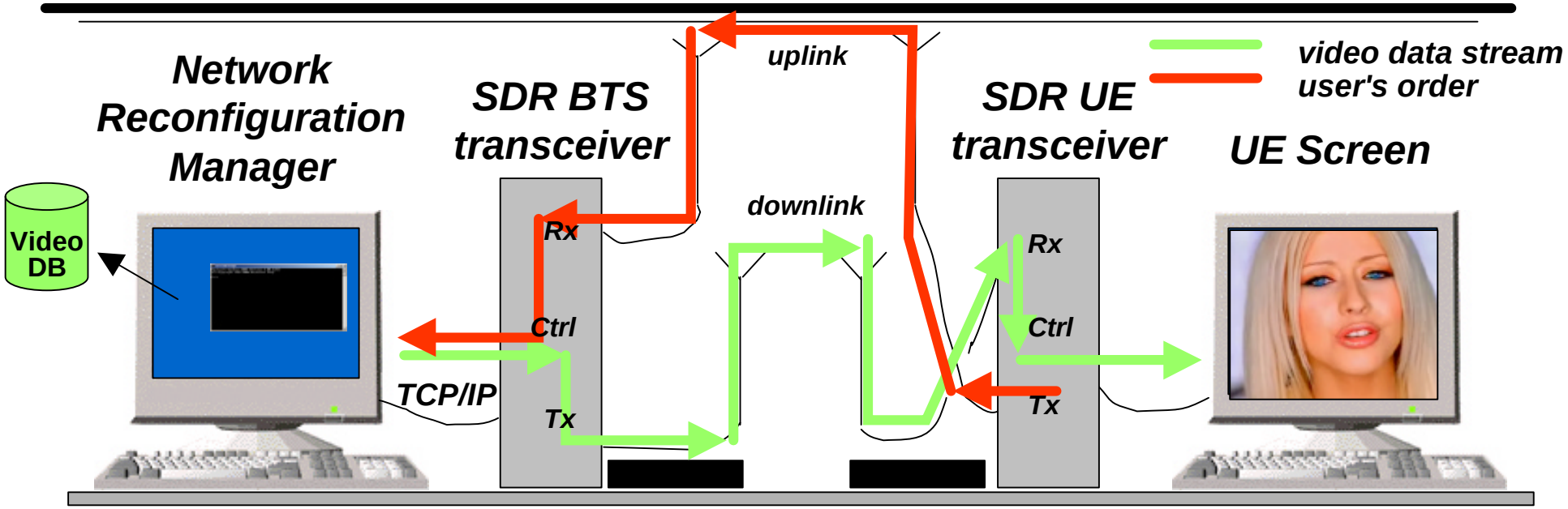


Network side

User Equipment side

Video application

TCP/IP over the air



- *Video service request from the user*

1 - the network has a video database

2 - launch a video server

3 - send the video stream to the BTS

4 - conversion of the stream to the reconfigurable EDGE protocol stack

5 - EDGE Tx

6 - EDGE Rx

7 - identification of the service

8 - video stream is displayed on the screen

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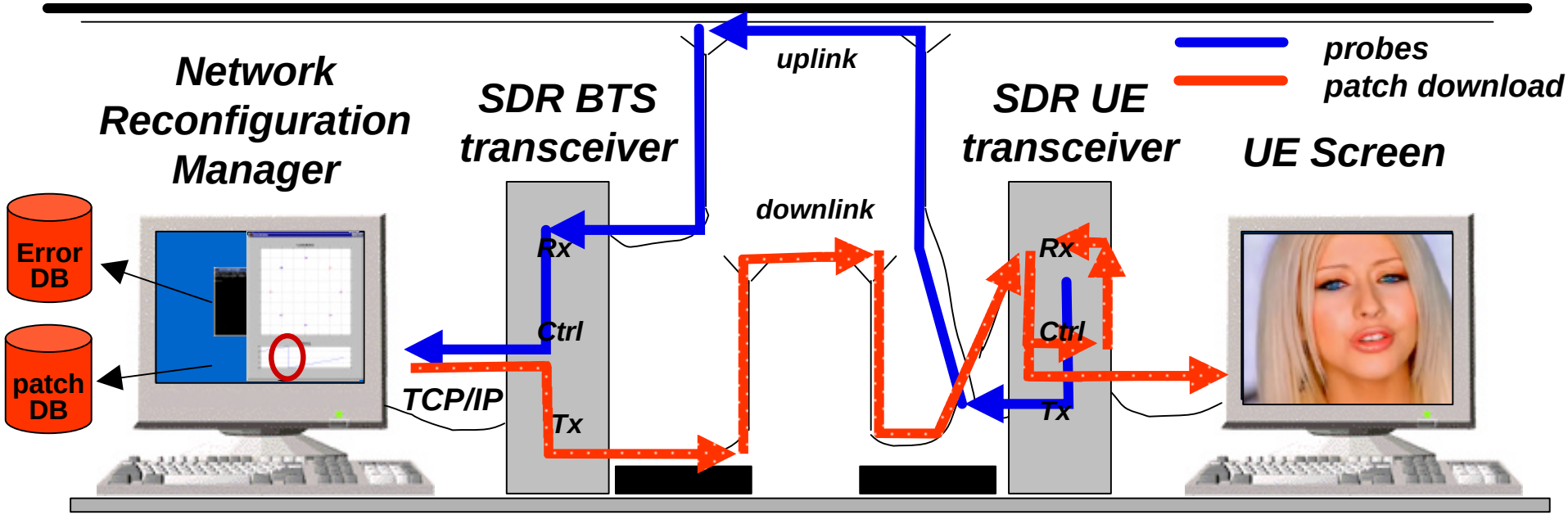
Reconfiguration at run-time

patch/upgrade download



Network reconfiguration manager

1 - monitors a SDR UE

2 - detects some dysfunction

3 - identifies the problem

4 - finds the corresponding patch in its patch database

5 - download the patch to the UE included in the data stream

6 - separate video from reconfiguration data

7 - install reconfiguration data in the UE's Rx internal memory

8 - activate the patch

9 - possibly: undo the operation if any problem

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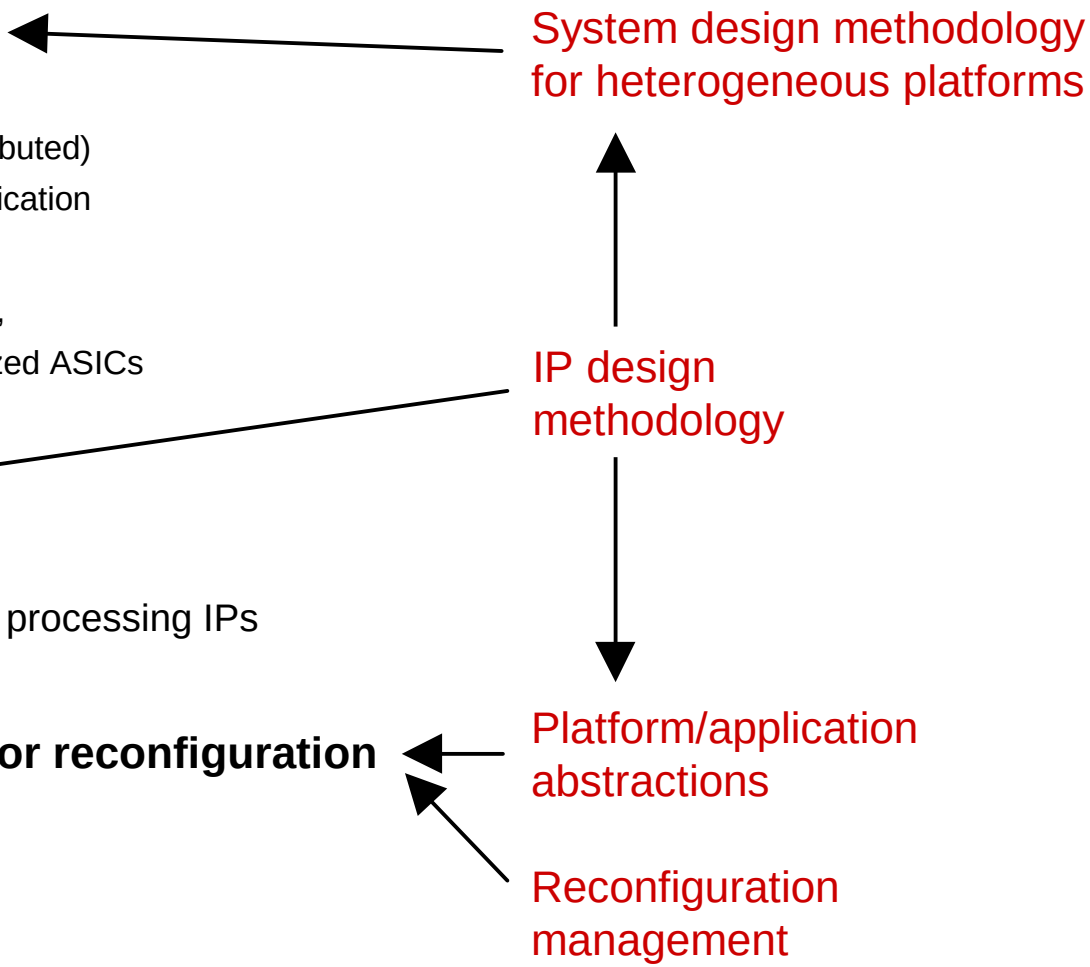
Requirements for reconfiguration

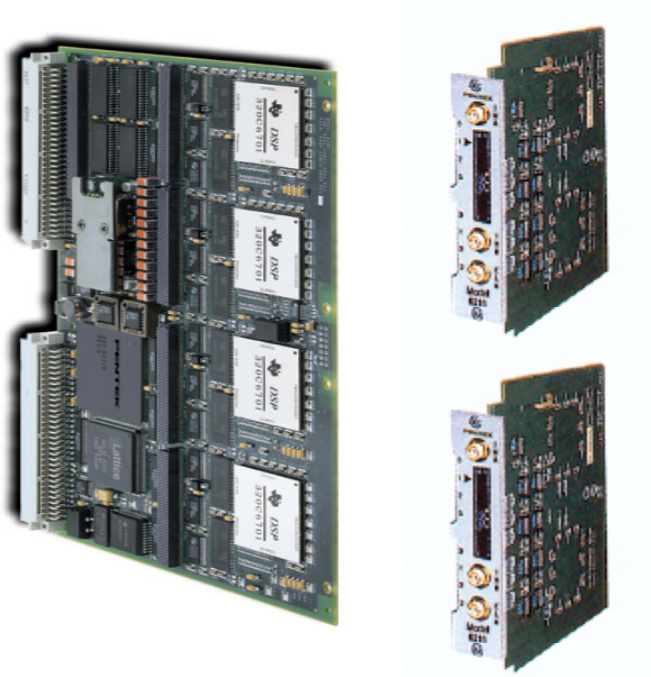
- **Req1: Hardware architecture**
  - computing power (potential)
    - multi-processing (SoC or distributed)
    - efficient internal data communication
  - reconfigurability (potential)
    - programable processors (SW),
    - reconfigurable HW, parametrized ASICs
- **Req2: Digital radio**
  - software signal processing IPs
  - reconfigurable hardware signal processing IPs
- **Req3: Software architecture for reconfiguration**



Req1: Hardware architecture

with emphasis on reconfigurability

- **multi-DSP mother-board**
  - 4 TI C6203 DSPs @300 MHz
  - high speed bi-FIFO comm links
  - host - target ethernet link (100 Mb/s)
  - supporting 2 daughter modules
- **2 channel wideband Tx module**
  - upconverter (DUC), D/A converter in IF
  - upconverter is bypassable
  - programmable parameters
- **2 channel wideband Rx module**
  - A/D converter in IF, downconverter (DDC)
  - downconverter is bypassable
  - programmable parameters
- **2 FPGA XC2V3000 Xilinx module**



possible digital IF

possible computing heterogeneity
DSP + FPGA
digital & analog param. ASIC

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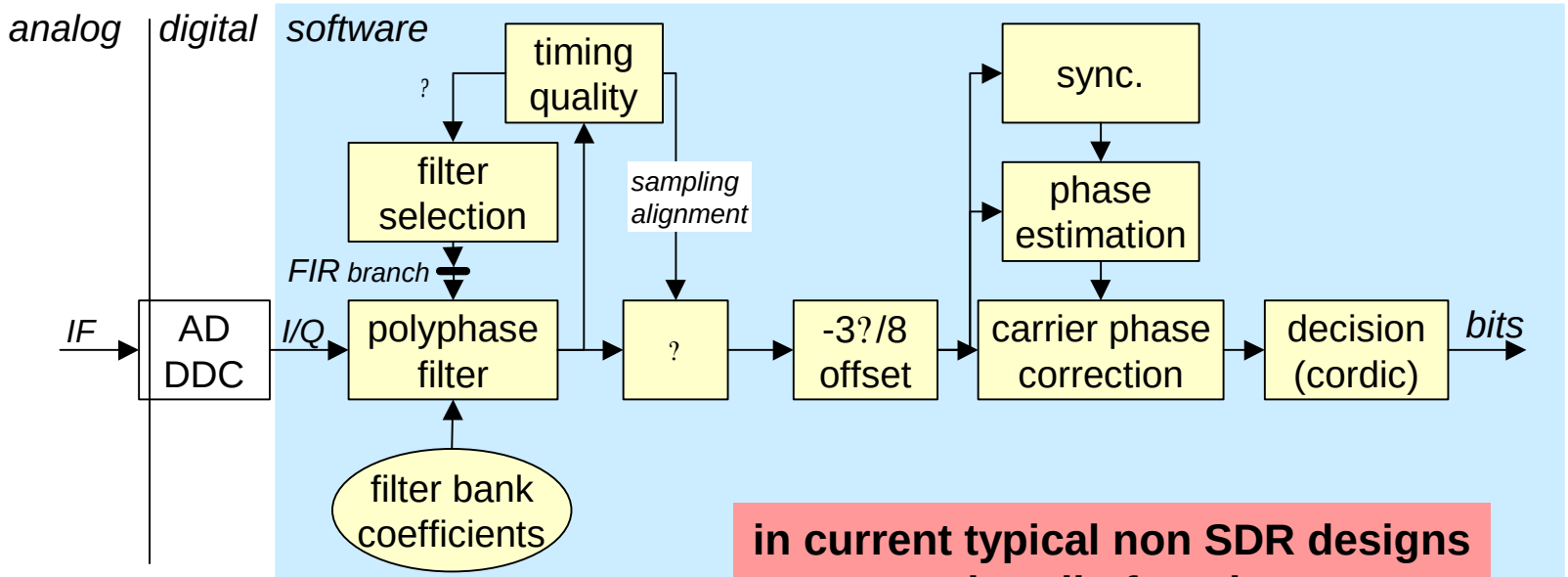
Req2: Digital Radio

example: EDGE receiver

- **digital-IF EDGE* receiver**



- **it has to be re-designed to enable dynamic reconfiguration of its parts; more to follow on this...**

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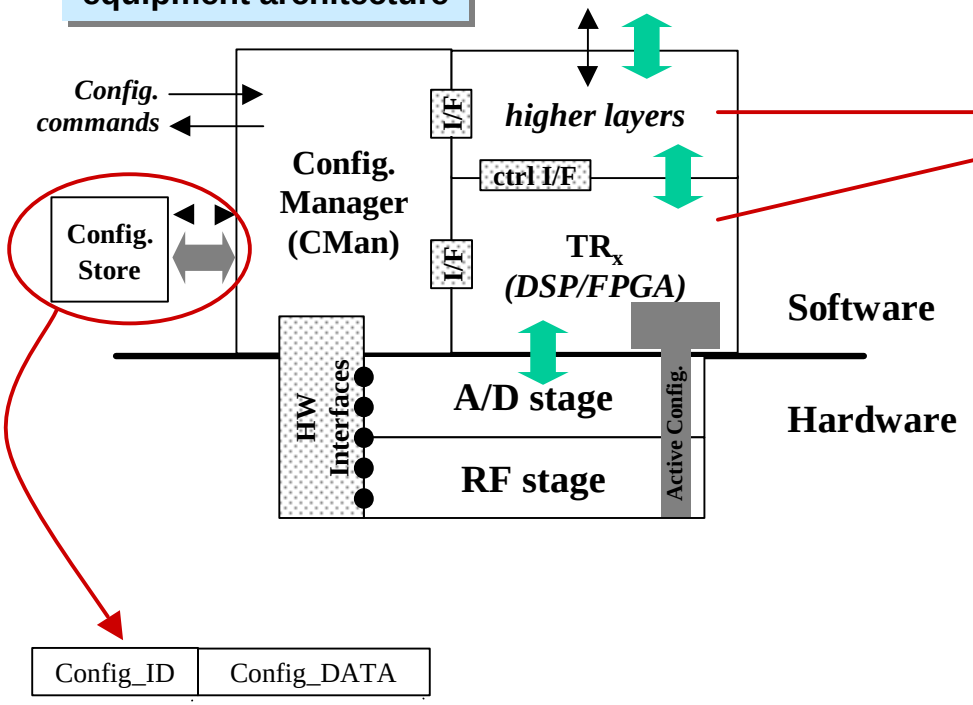
*EDGE (2.5G): Enhanced Data rates for GSM Evolution

Req3: Architectural & design issues for reconfiguration

equipment architecture



Config_ID	Config_DATA

HW parameters *scalar values*	SW parameters *scalar values*	SW functions *binary code*	HW functions *binary bitstream*	IO connections *pointer tables*

design approach

Component-based approach

"SW reconfigurable component"
implemented on programmable processors

"HW reconfigurable component"
implemented on programmable hardware
(e.g. FPGAs or parameterized ASICs)

reconfigurable component

Attributes

I/O Interface

Parameters

Methods

init()

run()

reconfigure()

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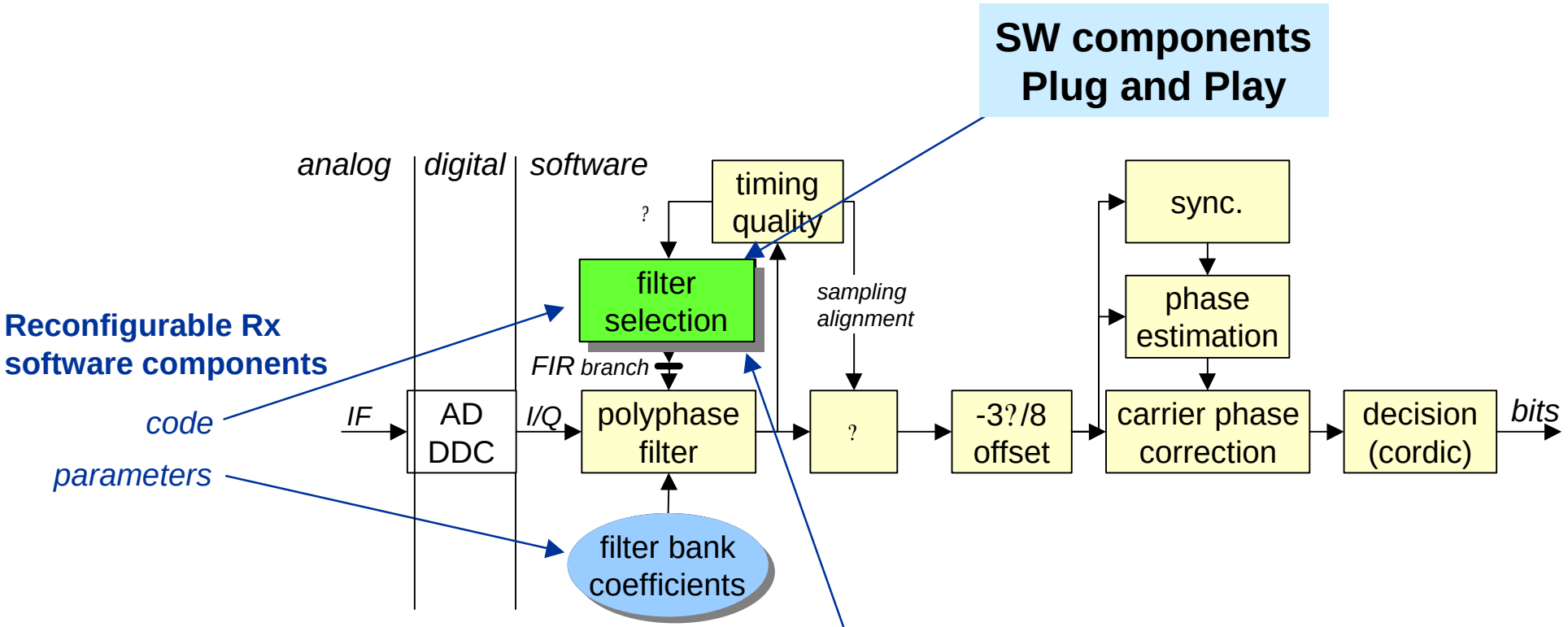
SWR component reconfiguration

- **Reconfiguration: reconfigure()**
  - for each component the equipment reconfiguration manager CMan calls the reconfigure method passing it the appropriate configuration data in a predetermined format
  - steps
    - configuration data is passed
      - new code and new parameters
      - function pointers for init, run are set to the desired implementations and a data pointer is set to the appropriate parameter structure understood by the implementations
    - init is called to setup internal state (optional)
    - run

Radio application software design

EDGE receiver re-design to enable dynamic reconfiguration



Filter selection function selects the right polyphase interpolating filter given a timing error estimation. This mechanism enables sub-sample timing recovery.

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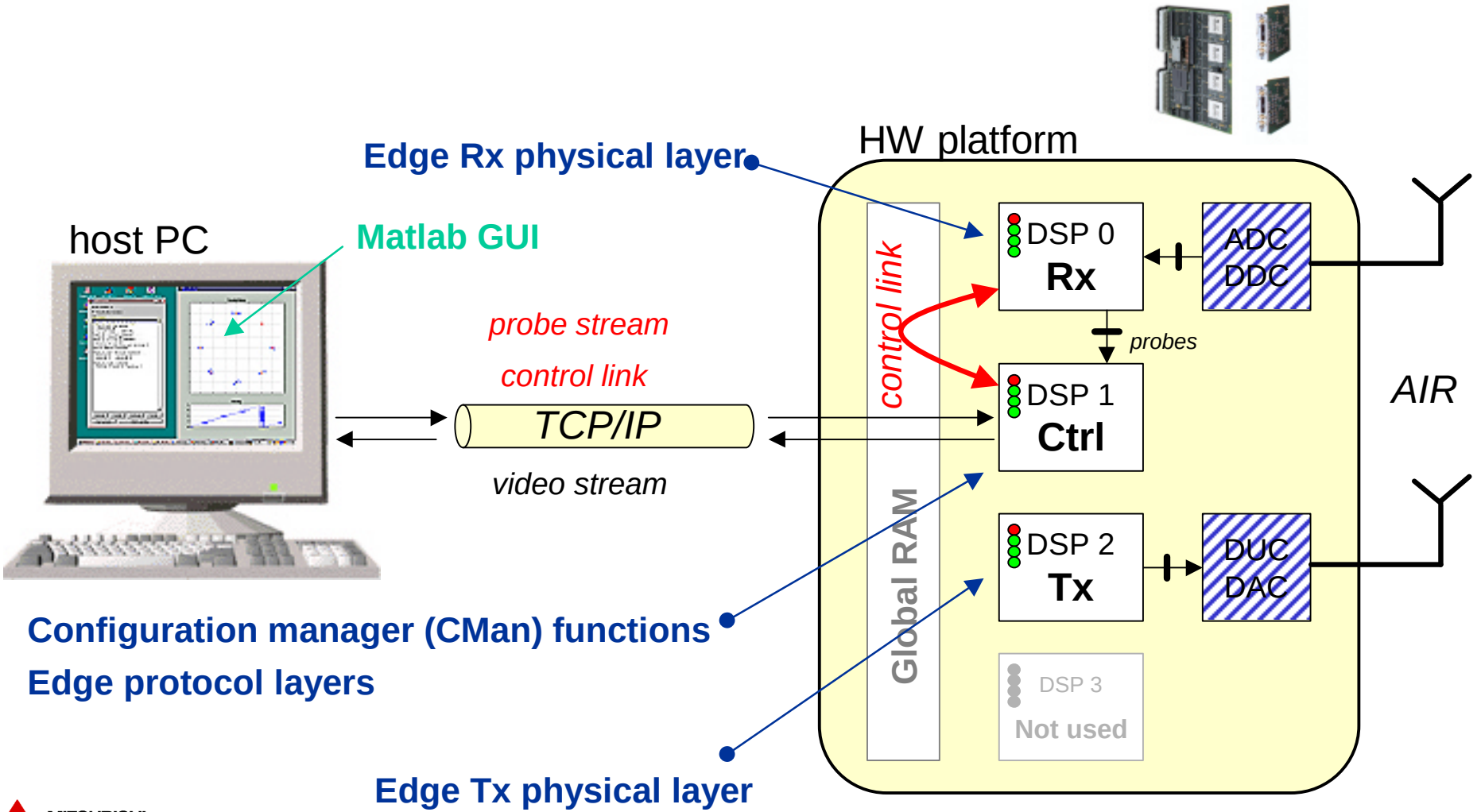
Reconfigurable SWR equipment

mapping of the radio application on the HW (including control)



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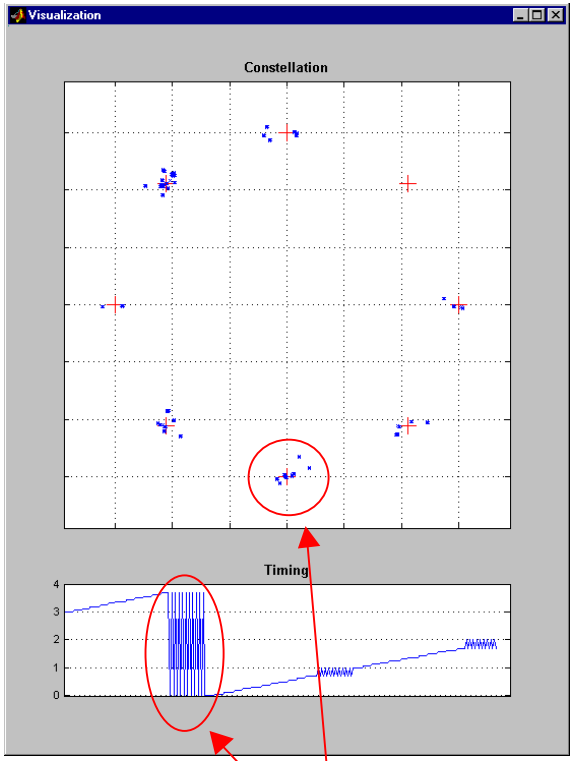
Reconfiguration process

- **3 steps approach**
  - download (may be skipped) / install / activate
- **Download**
  - if the reconfigurable system does not already have locally in memory the appropriate configuration data
- **Install: prepare a background execution context**
  - an installed configuration is stored in execution space but not diffused to the concerned components
- **Activate: switch execution contexts**
  - the active configuration is stored in execution space
  - parameter values have been diffused and code references have been resolved in the reconfigurable functional blocks

NRM GUI for reconfiguration management

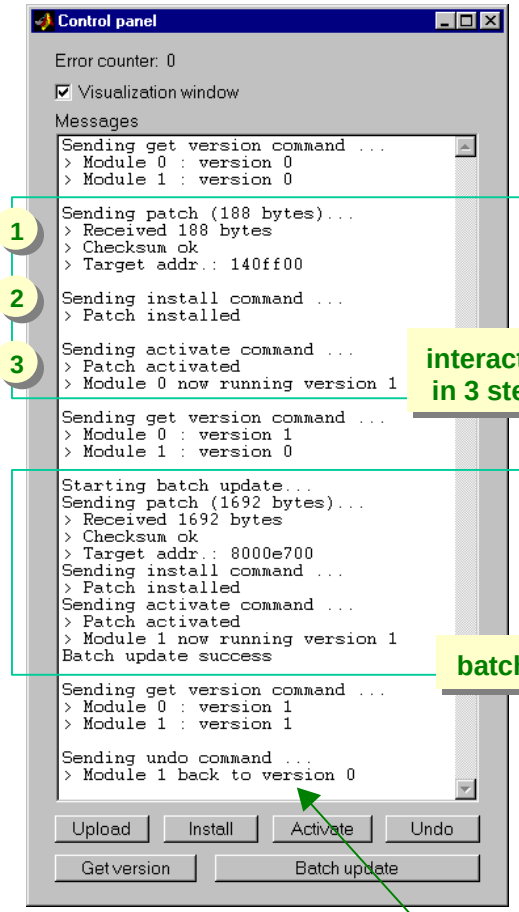
monitoring tool



no noise
sampling clock freq. drift

Bug in the Timing Recovery sub-system

reconfiguration controller

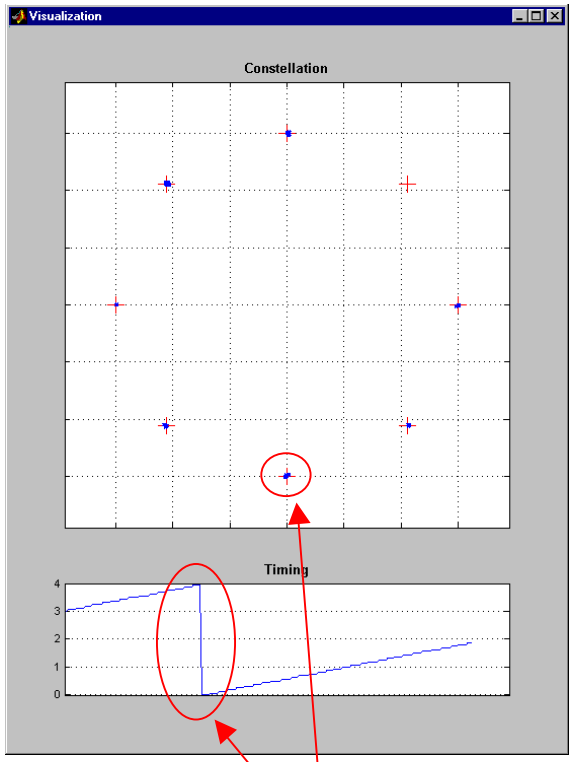


interactive in 3 steps

batch

rollback

monitoring tool



Bug corrected by selective code change, i.e. Module 0

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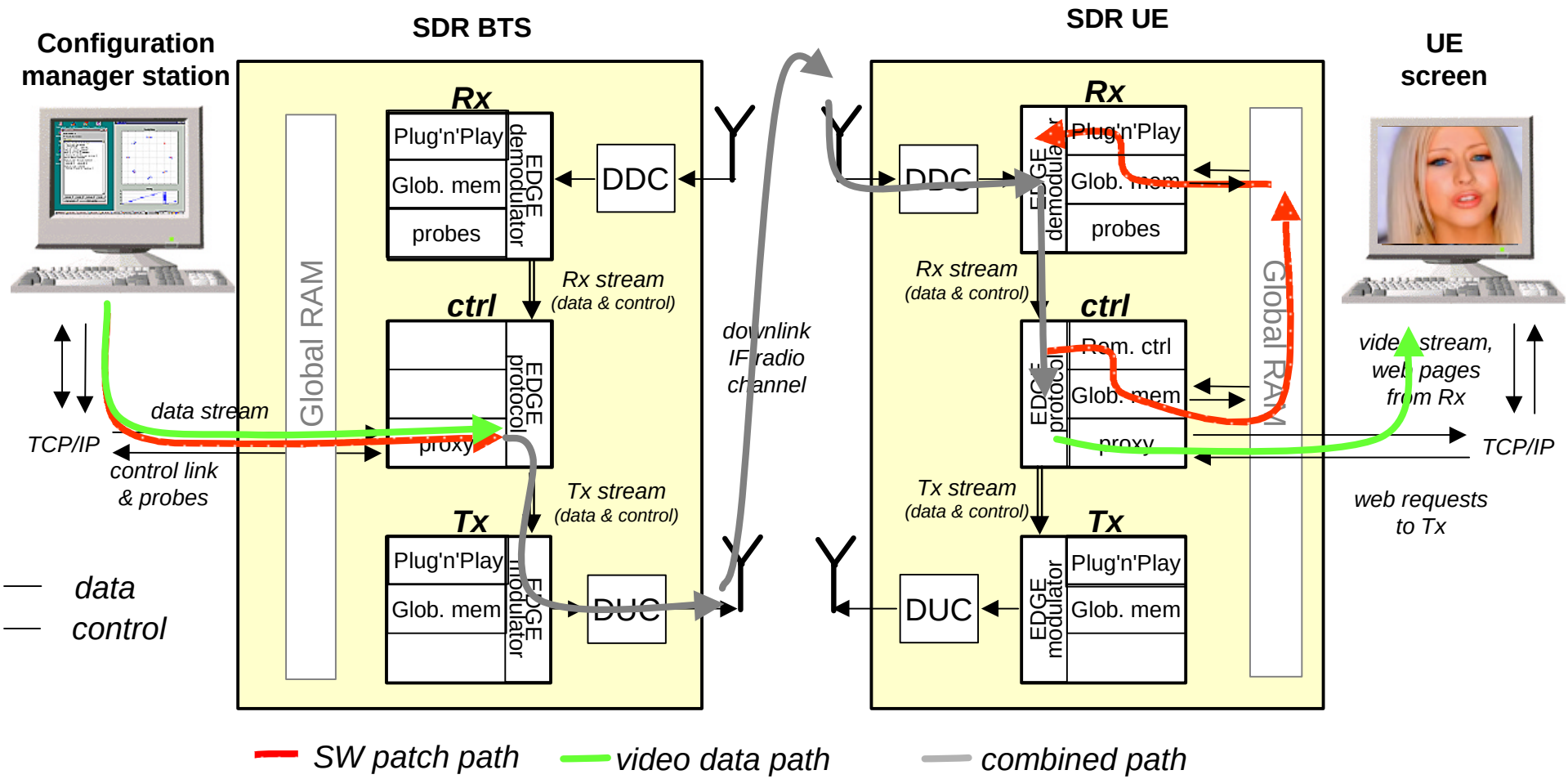
SW Patch path



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Real-time issues

- **only modules of potential interest are designed to be reconfigurable**
  - impact on a usual design may be very light
  - very low memory overhead necessary
  - permits a step by step deployment
- **small-size patch**
  - less than 0.5% of the overall code size
  - 4 kbits for the sampling time adjustment algorithm, 13 kbits for filter coef.
  - less than 0.5% of the processor cycles are needed
    - download + install < 50 ms (priority to signal processing)
- **keep former version in memory**
  - no need to download to back back to previous version if conditions are coming back to previous ones

Demonstration achievements

- **Successful proof-of-concept of a short-term reconfigurability application**
  - remote (i.e. over-the-air) run-time bug-fixing
- **Insight on equipment architecture and design principles**
  - component-based approach for hardware and software
  - configuration store, configuration manager
- **Reconfiguration procedure**
  - steps, reliability requirements
- **Insight on required network support**
  - message exchanges
  - intelligence distribution

a solid basis for further development has been established

Near-term perspectives

- **Efficient representation and manipulation of structure**
  - structural representation has to be enhanced, primitives (APIs) to operate changes in the structure
  - scenario description language
- **Reconfigurable HW (FPGA)**
  - reconfigure blocks located in FPGAs
  - partial reconfiguration
- **Include reconfiguration aspects in a high-level HW/SW co-design methodology**
  - automatically generate the different configurations
  - automatically generate the reconfiguration procedure
- **More complex reconfiguration scenarios**
  - algorithm switch with initialization & convergence phase
  - multi-mode, multi-standard
- **Reliability**
  - automated process with or without network involvement

Going further

- **Collaboration of the different actors is needed on a global scale**
  - academics, operators, regulators, manufacturers
- **Collaborative projects**
  - converge towards viable and universally acceptable solutions
  - e.g. E2R in Europe, TAO SDR in Japan (led by Mitsubishi)
- **International fora**
  - to build a common vision and consensus
  - e.g. WWRF, SDRF

to fully exploit the benefits from reconfigurability there are strong needs for standardization and regulation

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