#### Information Technology Center Europe Telecommunications Laboratory



a proof of concept by lab experimentation



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### **Outline**

- Mitsubishi Electric Telecom
- Motivations for Software Radio
- Motivations for reconfiguration
- HW generic platform
- 💉 Digital radio
- SW architecture for reconfiguration
- Z Demonstration
- *k* Roadmap
- Perspectives
- SDR projects
- Conclusion



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### Mitsubishi Electric Telecom

#### Mitsubishi Electric Telecom

- Motivations for Software Radio
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- **SW** architecture for reconfiguration
- Z Demonstration
- 💉 Roadmap
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### Mitsubishi Electric Telecom

#### Infrastructure

- PDC, PHS
- and future systems
- Mobile terminals
  - GSM/GPRS, PDC, i-mode, Foma (3G)
  - and future systems

Huge internal R&D effort on future wireless technologies

### Software Radio (SWR)

- Corporate R&D
  - labs in Japan, US and EU
  - Information Technology Europe:
    - VIL: Video and broadcast (UK)
    - TCL: Telecoms (France)
      - Software Radio department



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### **Motivations for Software Radio**

### 💉 Mitsubishi Electric Telecom

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### **Motivations for Software Radio**

#### A new way to design radio systems (both terminals and BTS)

- economic in the long term
  - mono-HW platform for several products
  - shorter design time (more SW design)
  - flexibility (last minute adaptation)
- easier to manage after selling
  - updates, bug fixing
- New radio capabilities
  - for the service providers' benefit
    - maintenance, service quality, performance enhancement (remotely)
  - answer users demand (for terminal)
    - personalization, differentiation
- A solution to multi-standard



### **Motivations for reconfiguration**

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### What is Software Radio?

- As much as possible of a radio system in digital and if possible in SW
- In order to benefit from the digital domain
  - design techniques
    - computer aided design tools...
  - technologies
    - low power, small size...
  - usual advantages for telecommunications
    - robustness, protection capabilities, capacity...

#### reconfigurability

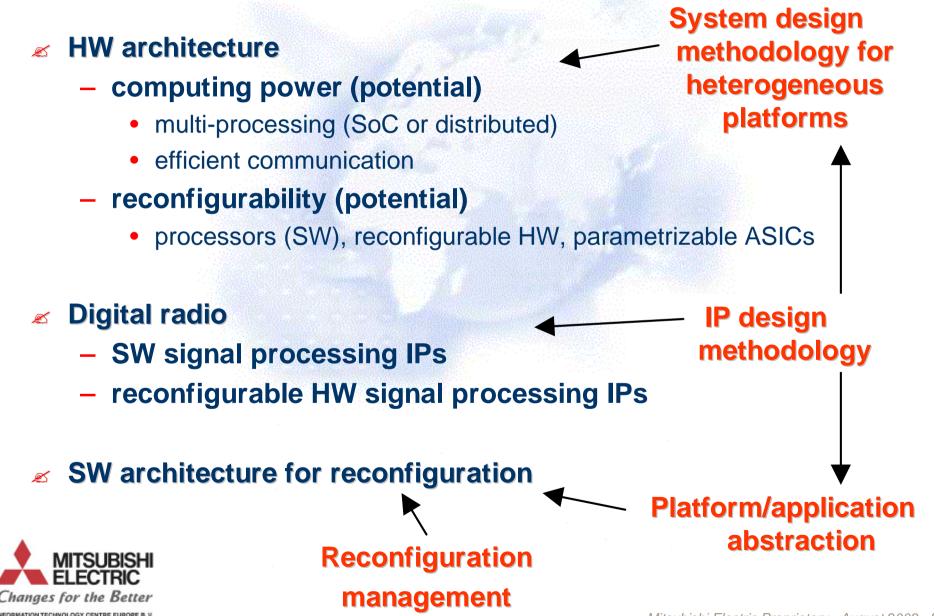
• processors, reconfigurable HW, parameterizable ASICs

Not only an evolution, but a new capability



### **Requirements for reconfiguration**

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## **HW generic platform**

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## HW generic platform requirements

#### *Genericity*

- many different applications are possible
- Heterogeneity
  - processors, reconfigurable HW, parameterizable ASICs
- Modularity
  - many daughter HW modules available, connectivity to outside world
- ✓ Scalability
  - third party boards may be added in the same rack
- Reconfigurability
  - thanks to processors, reconfigurable HW, parametrizable ASICs
- Portability
  - C language whatever processor, VHDL for reconfigurable HW
- SW co-design tools
  - automatic optimized mapping and code generation, HW/SW abstraction



### **HW generic platform**

#### multi-fixed point DSP mother-board

- 4 TI C6203 DSPs @300 MHz
- high speed bi-FIFO comm links
- host target ethernet link (100 Mb/s)
- supporting 2 daughter modules

#### 2 channel wideband Tx module

- upconverter (DUC), D/A converter in IF
- upconverter is bypassable
- programmable parameters

#### 2 channel wideband Rx module

- A/D converter in IF, downconverter (DDC)
- downconverter is bypassable
- programmable parameters

#### Z FPGA XC2V3000 Xilinx module

### possible digital IF







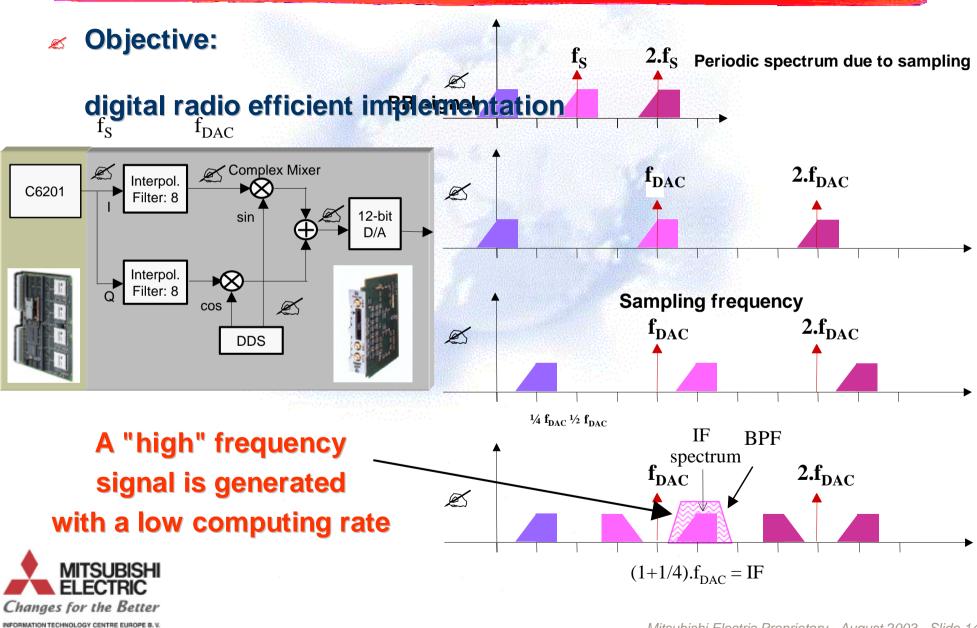
possible computing heterogeneity (DSP + FPGA + digital & analog param. ASIC)

# **Digital radio**

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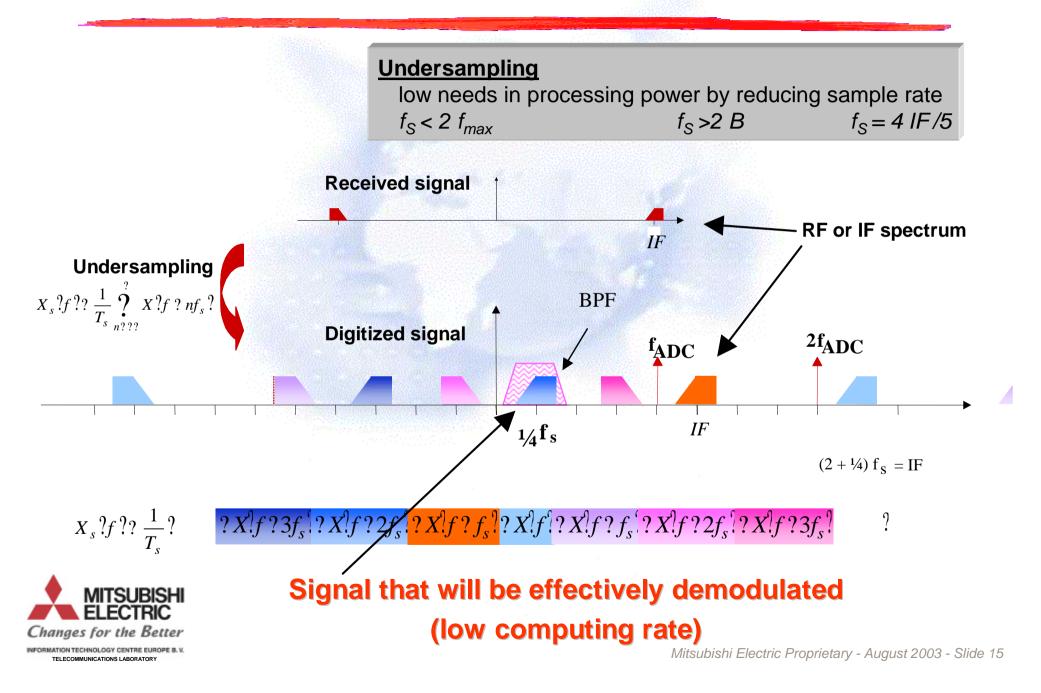


## "Undersampling" - Tx

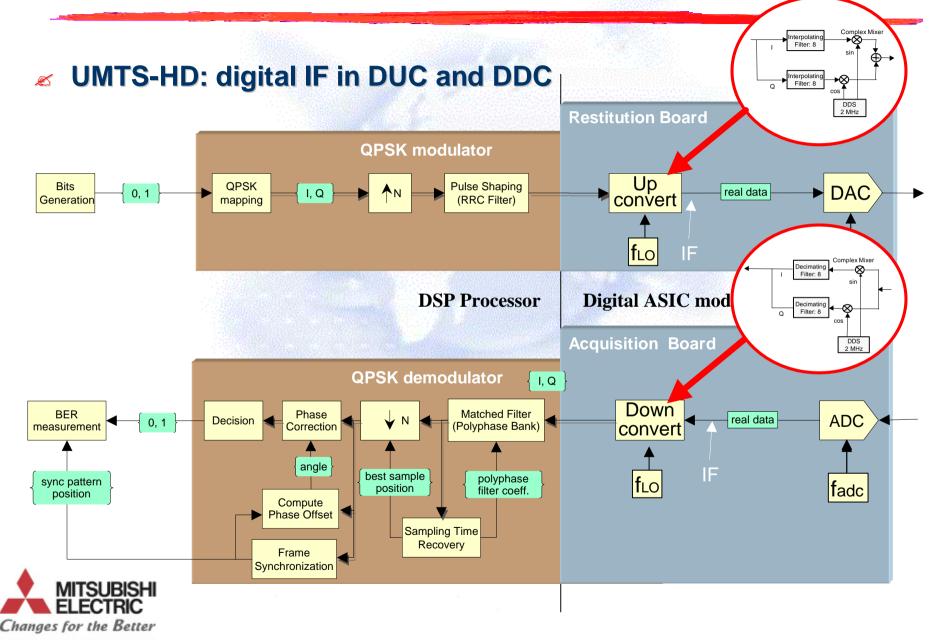


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### **Undersampling - Rx**

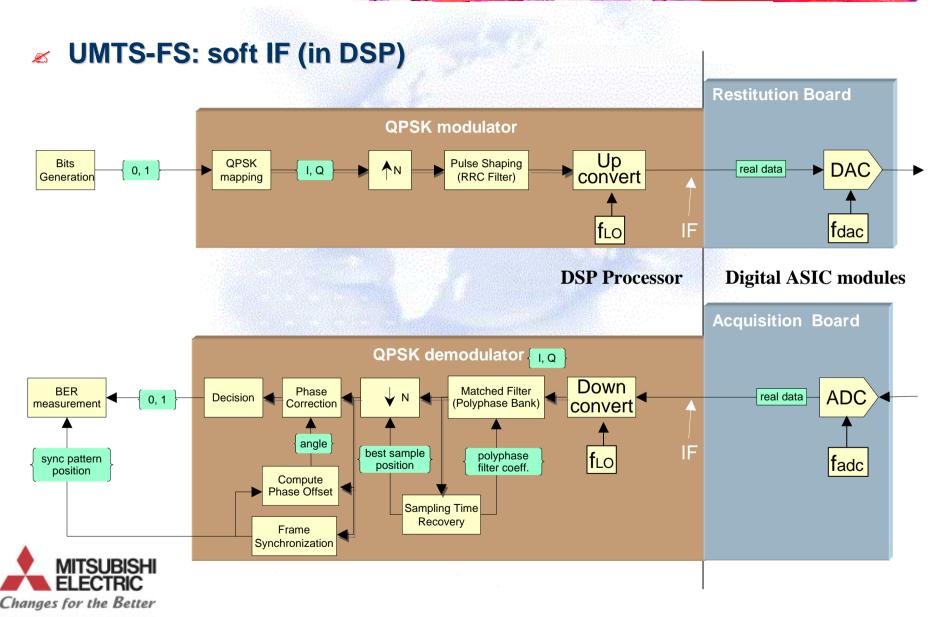


### **Digital IF - 3G UMTS FDD example**



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### **Digital IF - 3G UMTS FDD example**



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### Performance evaluation for a variety of transceivers\*

	Symbol ra	te 38/10	)	270 833	270 833	1000
Modem	Req. Perf. ksym/s	Tx Modulator		Rx Demodulator		1?s FH-CDM
		C6201 200MHz	C64x 1GHz	C6201 200MHz	C64x 1GHz	625 ? :
UMTS-HD	3840	960.8	4804	879.1	4395.5	1600 ho
UMTS-FS	3840	1434.2	7172	1435.3	7176.5	GFSK h: 0.28
GSM	270.83	444.6	2223	753.56	3767.8	0.35
EDGE	270.83	1036	5180	506.73	2533.65	
Bluetooth	1000	444.6	2223	825.49	4127.45	Gaussia BT: 0
						<b>D</b> 1: 0.
	(kbits/s)	144-20	000	9.6-13	< 384	1000

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### SW architecture for reconfiguration

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### SW architecture for reconfiguration

#### Component-based approach

- "SW reconfigurable component" on a processor
- "HW re-configurable component" on a FPGA or parameterizable ASIC
- A system is made of signal processing components with
  - their interconnections map ~
  - the behavior of each block
  - the parameters of each block

configuration information

structure implementation parameters

A reconfiguration is made through a configuration message containing all the configuration information of the blocks that are reconfigured



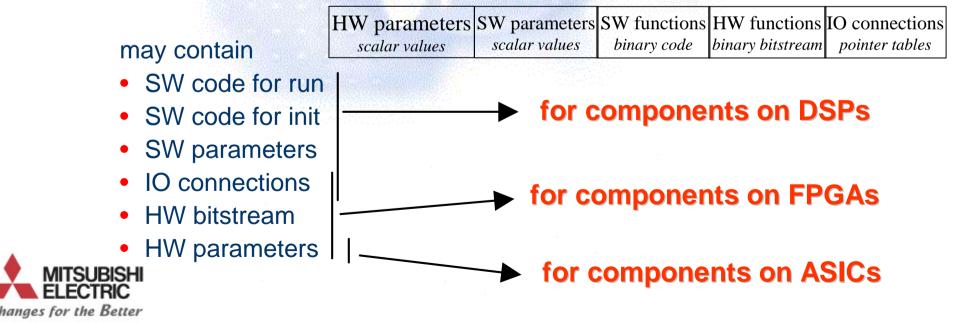
# **Configuration information exchange**

Configuration message

#### Configuration ID

- logical reference to the configuration DATA
- will be transformed to a physical reference by the configuration manager CMan

#### Configuration DATA



NFORMATION TECHNOLOGY CENTRE EUROPE B. V TELECOMMUNICATIONS LABORATORY Config ID

Config\_DATA

### **Reconfigurable components**

### Reconfigurable functional blocks

- I/O interface
- parameters
- implementation
  - init(), run()
- invariant function
  - reconfigure()

#### Reconfiguration: reconfigure()

- called by the configuration manager CMan
- steps
  - subset of configuration data is passed
    - new code or bitstream
    - new parameters
    - new I/O
  - function pointers for *init*, *run* are set to the desired implementations with the adequate parameters and connections
  - *init* is called to setup internal state (optional)
  - run



### **Reconfiguration process**

#### ✓ 3 steps approach

- download (may be skipped)
- install
- activate
- Z Download
  - if the reconfigurable system does not already have in memory the appropriate configuration

#### Installed configuration

stored in execution space but not diffused

#### Active configuration

- stored in execution space
- parameter values have been diffused and code references have been resolved in the functional blocks



### **Configuration cache**

1<sup>st</sup> level - configuration present in execution memory (L-CSt1)

- installed and ready for execution (after some init sometimes)
- reconfigure = software switching from one to another

#### 2<sup>nd</sup> level - configuration stored in the local global memory (L-CSt2)

- first bring configuration into execution memory (1<sup>st</sup> level cache)
- update configuration availability tables
- reconfigure (software switch)

#### **3**<sup>rd</sup> level - configuration stored in remote (network) site (R-CSt)

- download configuration into 2<sup>nd</sup> level cache
- install locally (1<sup>st</sup> level cache) & update configuration availability tables
- reconfigure (software switch)

#### does not systematically erase other present configurations

• several locations may be reserved in each cache for the same component



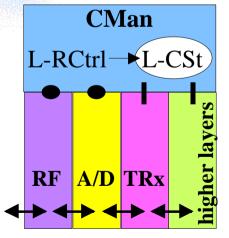
# **Example of a SWR User Equipment**

- Reconfigurable system 3 main entities
  - TRx: Transceiver
  - CMan: Configuration Manager
  - L-CSt: Local Configuration Store
    - contains the different configurations of all reconfigurable blocks
- 💉 CMan
  - interfaces with all reconfigurable sub-parts of the system
  - L-RCtrl: local reconfiguration controller
    - activates reconfigure()
    - manages the requests from the Network

**R-CSt** 

- monitoring requests from the network
- configuration information to the network
- consult the L-CSt
- HW interfaces for reconfiguration
- SW interfaces for reconfiguration
- ← data path

#### SWR UE

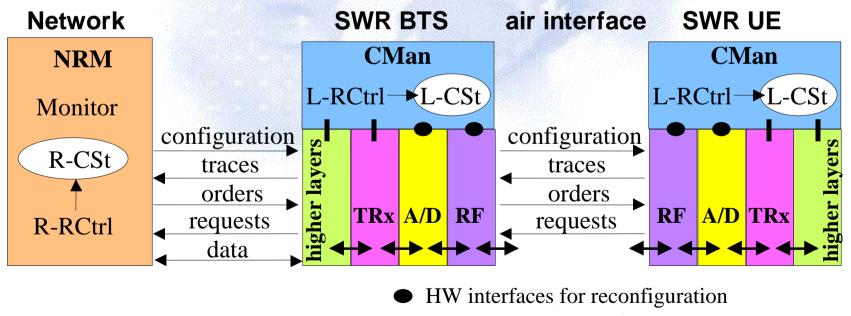


Changes for the Better

### **Network reconfiguration manager - NRM**

#### NRM manages reconfiguration

- operate monitoring tasks
- consult R-CSt: Configuration Store
- R-RCtrl: remote reconfiguration controller
  - initiates reconfiguration operation

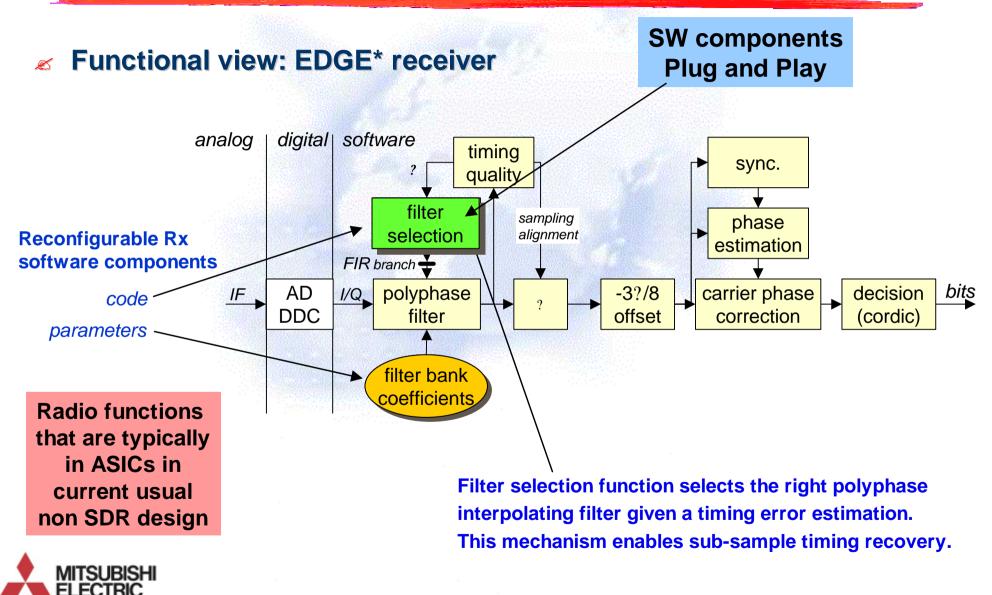




←→ data path

SW interfaces for reconfiguration

### Radio application SW design



\*EDGE (2.5G): Enhanced Data rates for GSM Evolution

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hanges for the Better

## **Case study: dynamic reconfiguration**

#### **SW** architecture appropriate for

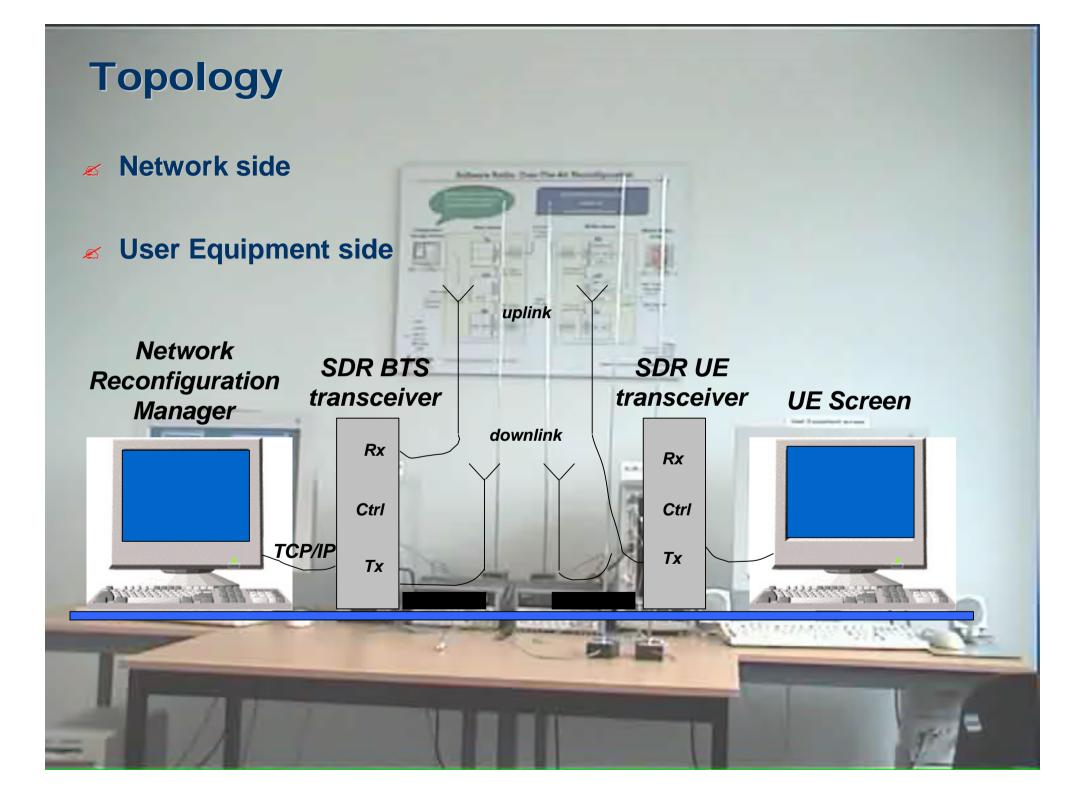
- heterogeneous systems
  - processors
  - FPGAs
  - parameterizable ASICs
- any functionality
  - physical layer
  - higher layers
- tested at the moment
  - on multi-DSP architecture
  - on physical layer algorithms
  - without structural changes
  - code and/or parameter download



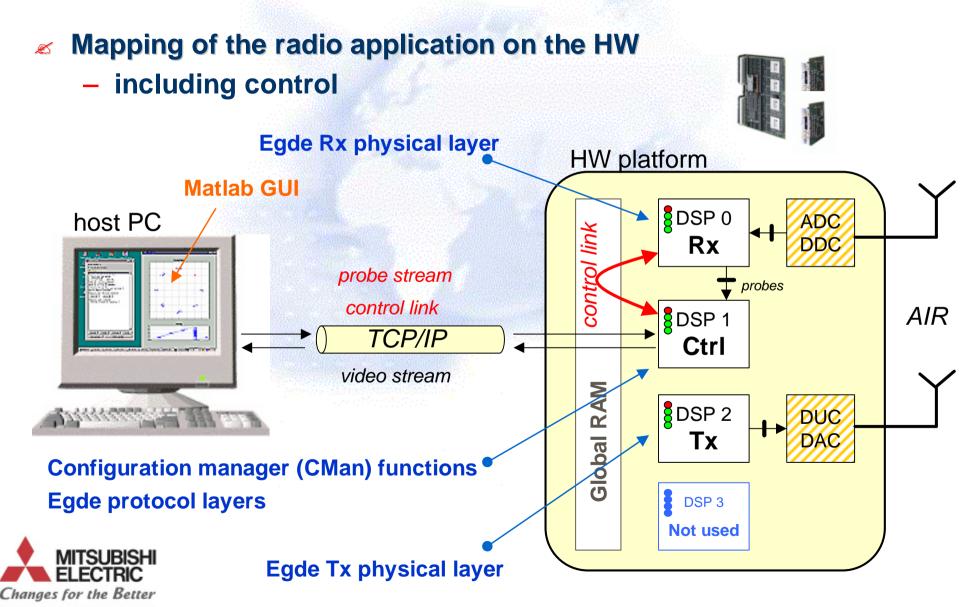
### **Demonstration film**

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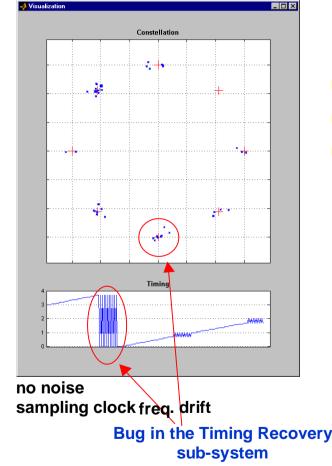


### Case study: dynamic reconfiguration

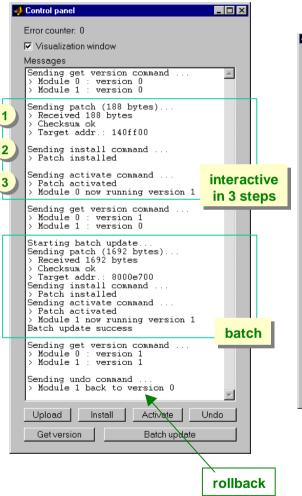


### **NRM GUI for reconfiguration management**

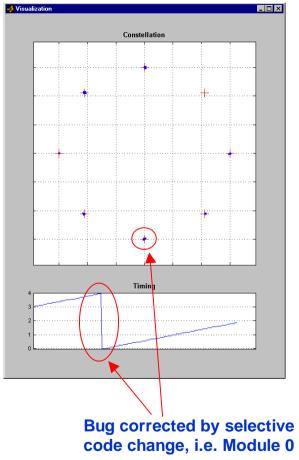
#### monitoring tool



#### reconfiguration manager

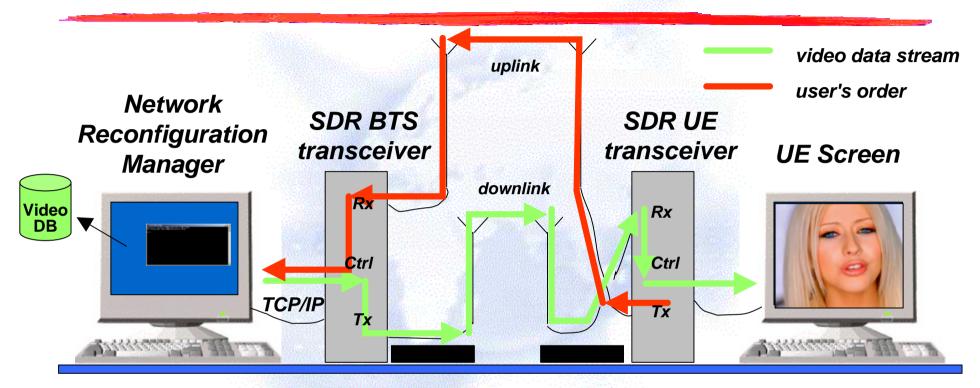


#### monitoring tool





### **Video application**



Video service order of the user

- 1 the network has a video database
- 2 launch a video server
- 3 send the video stream to the BTS
- 4 conversion of the stream to the reconfigurable EDGE protocol stack

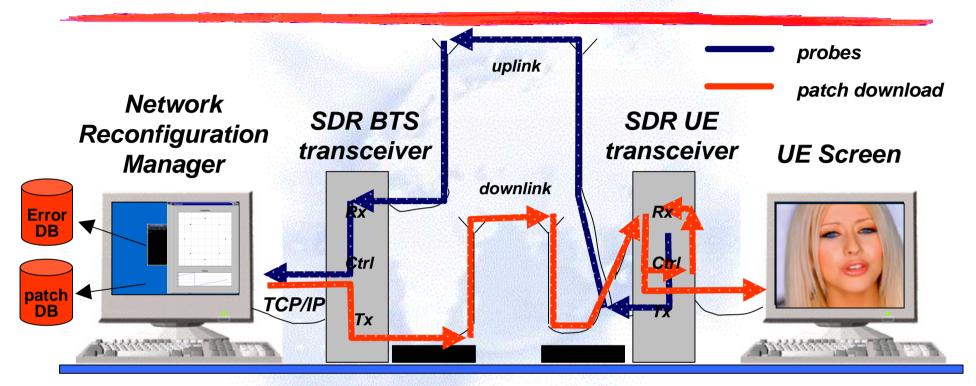
5 - EDGE Tx

- 6 EDGE Rx
- 7 identification of the service
- 8 video stream is displayed on the screen

TCP/IP over the air



### **Reconfiguration at run-time: patch download**



Network reconfiguration manager

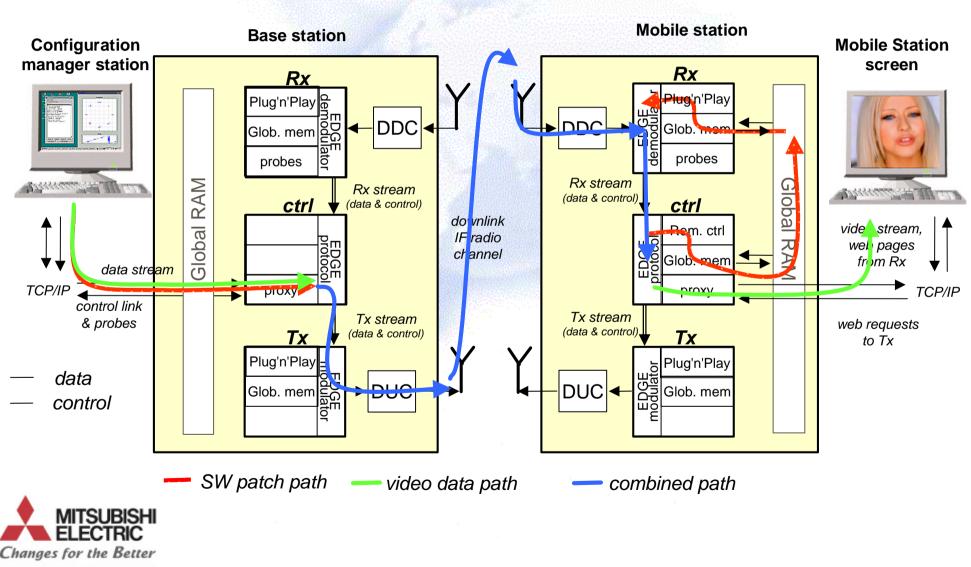
- 1 monitors a SDR UE
- 2 detects some dysfunction
- 3 identifies the problem
- 4 finds the corresponding patch





- 5 download the patch to the UE ;ircumstances included in the data stream new processing
- 6 separate video from reconfiguration data
- 7 install reconfiguration data in the UE's Rx internal memory
- 8 activate the patch
- 9 possibly: undo the operation if any problem

### **SW Patch path**

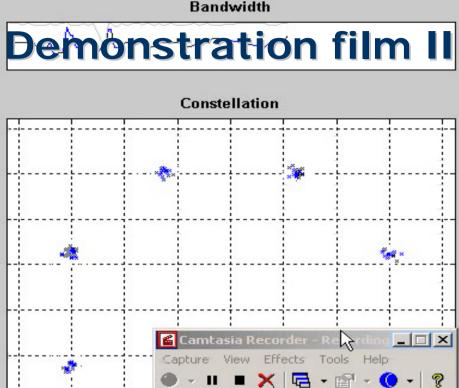


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### **Demonstration film I**

- Real-time reconfiguration of a EDGE transceiver at run-time
- Øver-the-Air SW download
- ✓ Bug fixing scenario
- Z During a video service transmission (no interruption)

### Bandwidth





# Messages **Screen capture** network side: monitoring panel reconfiguration control panel user equipment side: video Upload .Activate Install Undo Batch update Get version 🗑 ChristinaAquilera-250.wmv - Lecteur Windo... 💶 🗖 🗙 Fichier Affichage Lecture Favoris Allerà ? 4 ► II ■ 144 44 DF DF1 🗄

# **Real-time**

### only modules of potential interest are designed to be reconfigurable

- impact on a usual design may be very light
- very low memory overhead necessary
- permits a step by step deployment

### 3 steps download operation

- 3 cache levels
- using DMA capabilities

### ✓ small-size patch

- less than 0.5% of the overall code size
  - 4 kbits for the sampling time adjustment algorithm, 13 kbits for filter coef.
- less than 0.5% of the processor cycles are needed
- download + install < 50 ms (priority to signal processing)</li>
- keep former version in memory
  - no need to download to come back to former version
    - if conditions are coming back to previous ones



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# Roadmap

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- SW architecture for reconfiguration
- Z Demonstration

### 🗷 Roadmap

- Perspectives
- ✓ SDR projects
- 🥖 Conclusion



# Business cases for dynamic reconfig.

- Manufacturer
  - bug fixing
  - upgrade capabilities
- ✓ Service provider
  - bug fixing
  - performance enhancement
  - cell capacity optimization (transmit power adaptation)
- User may benefit in a transparent manner from
  - battery optimization
  - real-time quality of service management
- meeds for standardization and regulation



# **Technical feasibility roadmap (I)**

### Reconfiguration for remote software upgrades

Need agreement between OEMs, operators on: •what can be upgraded/changed •security, reliability, fault-tolerance, testing •how the upgrade/patch is packaged

### A1.1: remote upgrades as operator provided service A2: deployment of operator requested software upgrades

vare upgrades

several algorithms in the radio interface may be defined as upgradable in order to have the capability to enhance network performance and increase service quality operators may design their proper algorithms and then ask OEMs to provide the device software upgrades

•reconfiguration link & protocol
•needed network infrastructure

2003
A0: equipment design (preliminary phase)
generic HW platforms / differentiation in SW
user initiated switch/selection
mmode, multi-application by SW paging

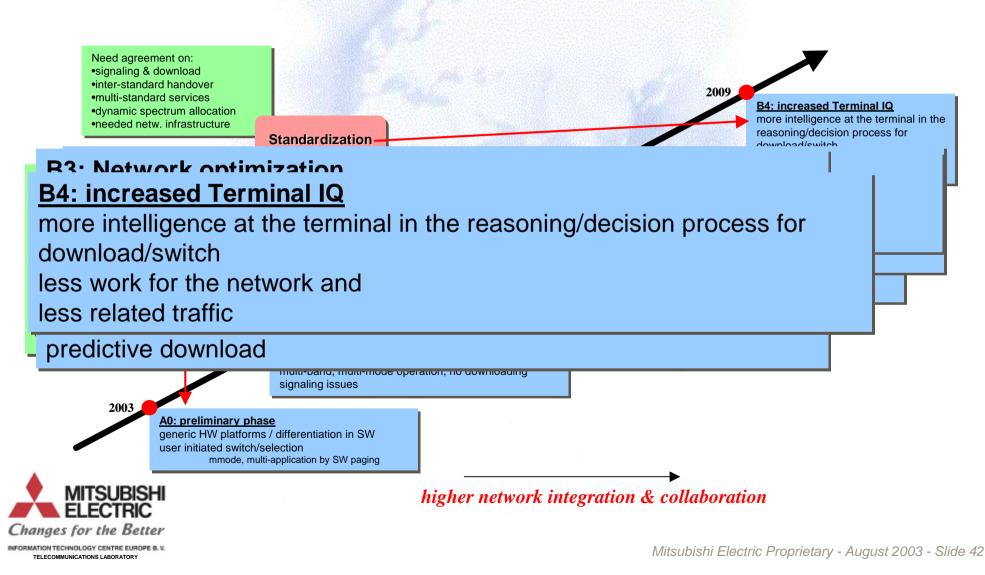
higher network involvement in the process



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# **Technical feasibility roadmap (II)**





# **Perspectives**

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# **Perspectives I**

### Conceptual level

- Structural changes
  - structural representation has to be enhanced
  - functions to operate changes in the structure
- Scenario description language
  - to deal with more complex reconfiguration procedures
  - automatic reconfiguration procedure deduced from changes nature

### Reconfigurable HW (FPGA)

- reconfigure blocks located in FPGAs
- partial reconfiguration
- Imply reconfiguration aspects in a high-level HW/SW co-design methodology
  - automatically generate the different configurations
  - automatically generate the reconfiguration procedure



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# **Perspectives II**

### More complex reconfiguration scenarios

- algorithm with initialization phase
  - former and new algo. run together until new algo converges
  - then switch
- multi-mode, multi-standard
  - with download or not
- Reliability
  - local initiative
    - UNDO initiated by the CMan after a timeout
  - remote initiative
    - some intelligence in the NRM manages the remote UNDO



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# ER: End-to-End Reconfigurability in EU

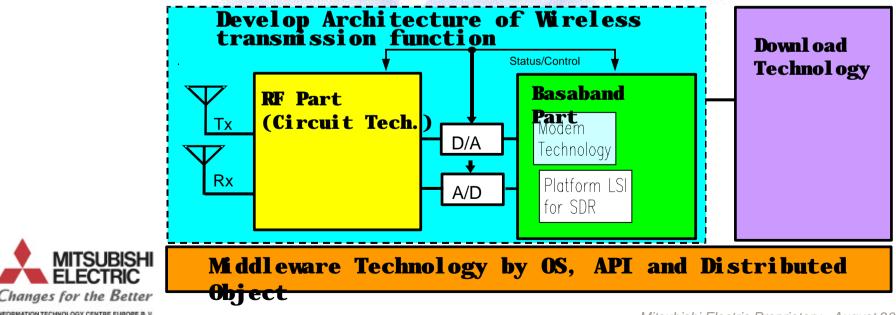
- IP project submitted to the European 6<sup>th</sup> Framework Program
- Work packages
  - WP1: System Research
    - technical, business and regulatory global approach across all WPs
  - WP2: Equipment Management
    - reconfiguration capabilities of equipments (terminal and BTS)
  - WP3: Network Support for Reconfiguration
    - network management for reconfiguring terminals and network entities
  - WP4: Radio Modem Reconfigurability
    - local configuration control and mechanisms for reliable reconfiguration
  - WP5: Evolution of Radio Resource and Spectrum Management
    - cognitive radio, network-oriented perspectives, spectrum control
  - WP6: E<sup>2</sup>R Proof of Concept Evolutionary Environment
    - demonstrator

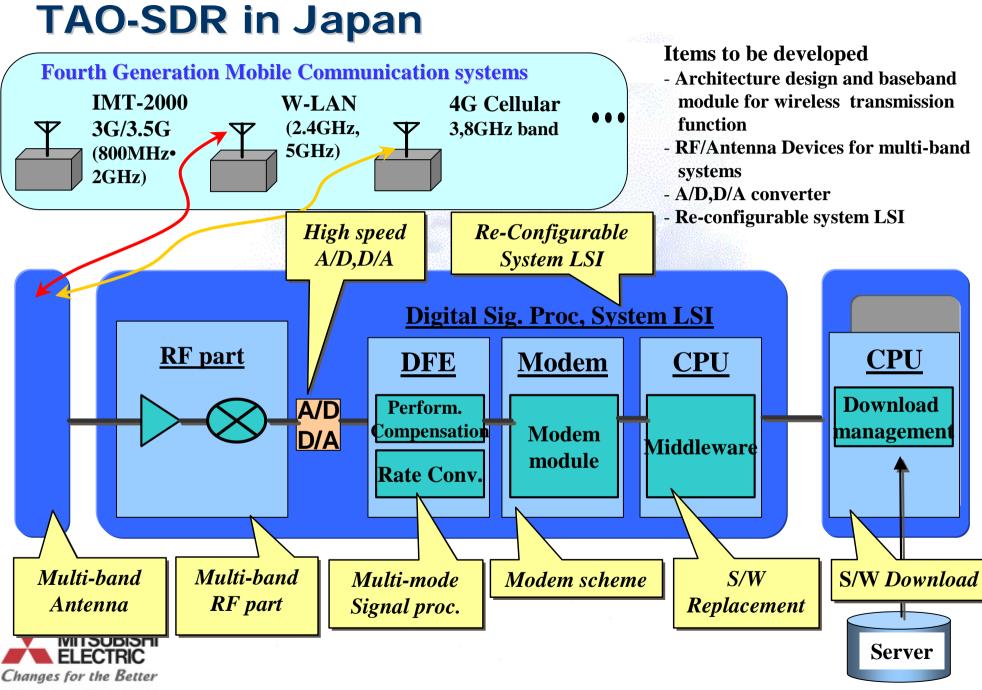
### **Some of the partners:**

MITSUBISHI Motorola, Siemens, Thales, Nokia, Mitsubishi, Panasonic, Alcatel, NTT ELECTRIC DoCoMo, Telefonica, FTR&D, UoAthens, UoSurrey, King's College...

# **TAO-SDR** in Japan

- Japan National Project
  - Mitsubishi Electric Japanese Lab (leader), Toshiba, Fujitsu
  - 4 years project (02 to 05)
- Øbjectives
  - R&D realization of 4G terminals with key SDR technologies
    - system architecture and devices for multi-mode/multi-band SDR terminal which supports 100Mb/s transmission rate and realizes seamless connection for multiple wireless systems





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# **Conclusion: keywords**

- Z Dynamic reconfiguration of a radio algorithm
- Øver-the-air SW download
- 😹 Bug fixing
- Performance enhancement
- At run-time of an application
- Code and/or parameter download
- **SW architecture** 
  - component-based
  - plug and play
- Laboratory demonstration

## Standardization and regulation effort are needed



# Conclusion

SDR Forum market survey by Gartner Consulting (jan. 2002)

### - for both US and EU wireless operators:

- "SDR technology will have a great benefit in fixing bugs in handset"
- "rapid SW bug fixing is expected to be a key value proposition for the handset market, especially as 3G emerges"
- "bug fixing is the clear top choice driven by the need to smooth the introduction of 2.5/3G services"
- Ø Operators will soon require dynamic reconfiguration for bug fixing
- Orange introduced in Oct. 2002 an Over-The-Air phone settings configuration (through SMS): "MyPhoneSettings" (from Swapcom)
  - 20.000 profiles are downloaded every day
  - Orange customer service that answers parameter settings issues saves 180.000 Euros each month



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